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Channel mobility in GaN hybrid MOS-HEMT using SiO_2 as gate insulator

Patrick Fiorenza, Giuseppe Greco, Ferdinando Iucolano, Alfonso Patti, and Fabrizio Roccaforte

***Abstract*—The channel mobility in SiO_2/GaN hybrid metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs) has been studied.. The formalism used for the inversion mobility in MOSFETs has been adapted to the case of GaN MOS-HEMTs, which operate in accumulation condition. Using the values of interface trapped charges (Q_{trap}=1.35×10^{12}cm^{-2}) and surface roughness (RMS=0.15nm) determined by capacitance-voltage measurements and nanoscale morphological analyses allowed to derive meaningful physical parameters for the mobility model. The temperature dependence of the peak mobility – that decreases from 110 cm^{2}V^{-1}s^{-1} at room temperature down to 91 cm^{2}V^{-1}s^{-1} at 423K – is mainly ruled by phonon and Coulomb scattering effects. The implications in practical devices were discussed, considering the possible improvement of the device on-resistance that can be obtained by reducing the interfaces state density at the SiO_2/GaN interface.**

***Index Terms*—AlGaN/GaN, channel mobility, Hybrid MOS-HEMT, SiO_2.**

I. Introduction

HIGH electron mobility transistors (HEMTs) on AlGaN/GaN heterostructures are attractive devices for high power and high frequency applications [1,2]. In particular, GaN-based power switches have been proposed for inverters and/or DC/DC converters in the electrified vehicles and renewable energies applications [3]. For power switching applications, normally-off AlGaN/GaN HEMTs are desired to guarantee the safety conditions required in many high power applications [3-6]. Several approaches to achieve normally-off HEMT have been proposed, like the recessed gate process [7], the fluorine incorporation via plasma etch under the gate [8], the surface oxidation process [9], the use of a thin AlGaN barrier layer [10], or the use of a p-(Al)GaN gate [11-13]. In the recessed gate approach, although the reduction of the barrier layer thickness, by selective plasma etching, leads to a positive shift of the threshold voltage V_{th} [14], the control of the etching rate uniformity on a large area can be critical. To overcome this technological issue, the hybrid MOS-HEMT configuration has been proposed [15], in which the complete removal of the AlGaN barrier has a better reproducibility on large area GaN wafers up to 8" wafers (on silicon) [16]. Basically, the hybrid MOS-HEMT concept consists in the local replacement (in the gate region) of the AlGaN barrier layer with a gate insulator. In this way, the advantage of a normally-off MOS-channel is added to the low-resistance offered by the two dimensional electron gas (2DEG). Basing on this concept, devices with positive threshold voltage (up to +2V) and R_{on}<10mΩcm^2, suitable for operation in the kV range, have been demonstrated [17,18].

In a hybrid MOS-HEMT, the most critical building block is the recessed channel region, where surface roughness and/or electrically active defects can have an impact on the channel mobility. *Ki-Sik, et al.* [19] reported an excellent value of channel mobility (up to 225 cm^{2}V^{-1}s^{-1}) using Al_2O_3 as gate dielectric. On the other hand, *T. Oka and T. Nozawa* [20] demonstrated MOS-HEMTs employing SiN as gate dielectric, with a high threshold voltage (V_{th}> 4V) and high breakdown voltage (>400V). Clearly, in this context, the comprehension of the mechanisms ruling the channel mobility and its temperature dependence are fundamental to pave the way for further improvements of MOS-HEMT devices performances, and still need to be deeply investigated.

Several papers reported on the temperature dependence of the characteristics of planar MOS-HEMTs (i.e., with an "insulated gate" but without recession), compared to standard HEMTs (i.e, with a Schottky barrier gate) [21-23]. In particular, Liu *et al.* [21] demonstrated better dc performances and thermal stability of planar MOS-HEMTs with an Al_2O_3 layer formed by the H_2O_2 oxidation of the substrate with respect to conventional ones (i.e., using a simple Schottky gate). *Pérez-Tomás et al.* [22] proposed a model to describe the temperature dependence of the inversion channel mobility in GaN MOSFETs, pointing out that, while at lower temperatures (T ~ 300-350 K) the channel mobility is limited by the Coulomb scattering, the surface roughness becomes relevant for increasing values of T (>400K) [22]. In the case of normally-on AlGaN/GaN HEMTs operating at elevated T, the same group [23] demonstrated that the decrease of the mobility with increasing temperature is due to the dominant contribution of the polar-optical-phonon mobility of the free carriers moving in the 2DEG. Finally, while few papers simulated the temperature dependence of the channel mobility

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in recessed hybrid MOS-HEMTs [24,25], an exhaustive correlation between mobility model and experimental data in hybrid MOS-HEMTs has not been reported yet.

In this paper, the channel mobility in GaN-based hybrid MOS-HEMTs has been studied and correlated to experimental electrical and morphological analyses performed on the channel region. The common MOSFETs mobility formalism has been adapted to the case of GaN MOS-HEMTs, which instead operate in accumulation condition. The results have been discussed considering the potential improvement of the channel mobility and of the on-resistance that can be obtained in practical devices by a further optimization of the electrical properties of the insulator/GaN interface.

II. Experimental

SiO_2/GaN recessed hybrid MOS-HEMTs and MOS capacitors fabricated on the same wafer were used. Commercial $Al_{0.25}Ga_{0.75}N$/GaN heterostructures grown on p-type Si(111) substrates with a resistivity < 30mΩ/cm were used. The GaN layer has a low nominal doping concentration of $N_D \approx 10^{15}$cm^{-3}. The AlGaN layer recession was carried out by an atomic-layer-etch (ALE) using a Chlorine-based chemistry [26]. As gate insulator, a 50 nm thick SiO_2 layer was deposited by plasma enhanced chemical vapour deposition using tetraethyl orthosilicate (TEOS) precursor, and subjected to a thermal annealing at 850°C in N_2. Ti/Al-based metallization annealed at 550°C was used for source and drain Ohmic contacts [27] and Ni-based for the gate contact (Fig.1). Normally-off hybrid GaN MOS-HEMTs with an appropriate FAT-FET geometry (channel length L=40µm, channel width W=200µm, distance of the gate from source/drain contacts $d_{sg} = d_{gd}$ = 8µm) were used to minimize the resistive contribution of the access regions, down to about 2% of the total series resistance.

The electrical characterization of the devices (both MOS-capacitors and MOS-HEMTs) was carried by capacitance-voltage (C-V) measurements and current-voltage (I-V) at different temperatures, using a Cascade probe station and an Keysight B5105 parameter analyzer.

The morphology of the MOS-HEMT channel region (i.e., the GaN surface in the recessed region) was investigated using a PSIA XE-150 Atomic Force Microscope (AFM) operating in non-contact mode with highly doped silicon tips. These measurements were carried during the fabrication flow of the devices, i.e., before the gate oxide deposition step.

III. Results and Discussion

Fig. 1 shows the transistors I_{DS}-V_{DS} characteristics (a) and I_{DS}-V_{GS} transcharacteristics both in semi-log and linear scale (b). The threshold voltage was determined by the linear extrapolation of the $\sqrt{I_{DS}}$ vs V_{GS} plot. (V_{th} = +0.7V).

The study of the temperature behaviour of the field effect

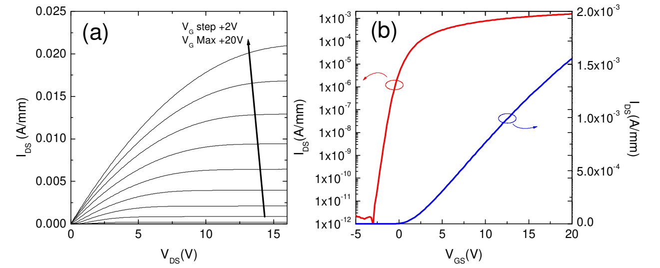

Fig. 1. (a) I_{DS}-V_{DS} characteristics (a) and I_{DS}-V_{GS} transcharacteristics both in semi-log and linear scale (b).

mobility (μ_{FE}) is a useful method to get information on the insulator/semiconductor interface properties in MOSFETs. The μ_{FE} was derived from the transconductance in the linear region (i.e., the derivative of the I_{DS} -V_G curve at constant drain voltage V_{DS}=0.5V), according to the expression:

$$\mu_{FE} = \frac{L}{WC_{ox}V_{DS}}\left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \tag{1}$$

where C_{ox} (C_{ox}=5.53×10^{-8} F/cm^2) is the insulator capacitance per unit area, L is the channel length, W is the channel width, V_D is the drain voltage.

Since the series resistance of the access regions could lead to un underestimation of the channel mobility, its contribution was minimized using FAT-FET devices of appropriate L/W geometry (see Section II). Under these conditions, it is possible to use the standard MOSFET formalism.

Fig. 2 shows the experimental values of the field effect mobility μ_{FE} as function of $V_G - V_{th}$ at different measurement temperatures (25-150°C). In this temperature range V_{th} slightly increased by increasing the temperature with a slope of 1.6mV/K. As can be seen, the maximum of these curves (peak mobility) decreases with increasing the measurement temperature. The temperature dependence of the peak mobility will be discussed in section E. It has to be mentioned that the sub-threshold region of the I_{DS}-V_{GS} can be affected by the non-steep change in the gate-capacitance. As a consequence, the early ascending part of the field effect mobility vs V_G-V_{th} (Fig. 2) can be influenced by the soft gate-capacitance variation. However, for V_G-V_{th}> 2V the device is in accumulation with almost constant capacitance value. Hence, the peak mobility values used in the following part of the manuscript are not affected by the capacitance value variation.

Recently, some authors described the channel mobility on MOSFETs fabricated on wide band gap semiconductors [22,23,28,29] considering different contributions in the Matthiessen's rule, i.e., the bulk mobility factor (μ_B), the acoustic-phonon scattering (μ_{AC}), the surface roughness scattering (μ_{SR}), and the Coulomb scattering (μ_C) due to the presence of interface charges:

$$\mu_{FE} = \left(\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C}\right)^{-1} \tag{2}$$

In the following sections, the single contributions entering

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in Eq. (2) are discussed.

A. *Bulk Mobility*

The temperature dependence of the bulk mobility component μ_B can be expressed using the model proposed by Caughey and Thomas [30]:

$$\mu_B(T)=\mu_{min}+\frac{\mu_{max}\left(\frac{T}{300}\right)^{-\beta_1}-\mu_{min}}{1+\left\{N_D\times\left[N_{REF}\left(\frac{T}{300}\right)^{\gamma}\right]^{-1}\right\}^{\lambda_1}} \quad (3)$$

where T is the absolute temperature and N_D is the doping concentration of the material.

The term N_{REF} $(T/300)^{\gamma}$ in Eq. 3 varies from 3×10^{17} to 1×10^{18} cm^{-3} in the temperature range of interest (298-423K). According to Eq. (3), for a doping level lower than $10^{16}cm^{-3}$ the bulk mobility saturates at about 1600 cm^2/Vs..Hence, due to the lower doping concentration of the GaN substrates used in the present work ($N_D \approx 10^{15}cm^{-3}$), one can assume μ_{max} = 1600 cm^2/Vs. Accordingly, the temperature dependence of the bulk mobility contribution was calculated with Eq. 3, using the other parameters (N_{REF}, μ_{max}, μ_{min}, β_1, γ, λ_1) determined for GaN by Vitanov and Palankovski [31] and reported in Table I.

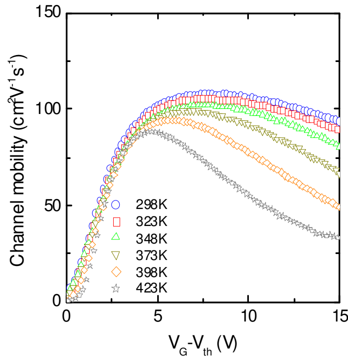

Fig. 2. Field effect mobility μ_{FE} as a function of V_G-V_{th} at different temperatures.

B. *Phonon Scattering*

In GaN polar semiconductor, the phonon scattering is given both by acoustic and optical phonons. However, in our hybrid GaN MOSHEMT device, the 2DEG is not present in the channel region, owing to the complete removal of the AlGaN barrier. Hence, the situation is analogous to the channel of a GaN MOSFET. In this condition, optical phonon scattering is typically shielded by the presence of GaN/insulator interface traps [22] and, hence, only acoustic phonon are considered.

The surface acoustic phonons mobility coming from the quantized mode of vibration occurring in the crystal lattice has been given by Lombardi *et al.* [32]:

$$\mu_{AC}(T;E_\perp)=\frac{B}{E_\perp}+\frac{CN_D^{\alpha_1}}{TE_\perp^{1/3}} \quad (4)$$

This expression allows to describe the mobility reduction due to the electric field normal to the current flow as a function of both the orthogonal component of the electric field *($E_\perp$)* and of the temperature (*T*). For the case of GaN MOSFETs, the parameters *B, C* and α_1 have been obtained by Pérez-Tomás et al. [23,33] and their values are reported in Table I.

It is worth noting that the expression of μ_{AC} given in Eq. (4) has been developed for a lateral MOSFET working in inversion mode, i.e., the n-type electron channel is formed on a p-type semiconductor under a appropriate reverse bias conditions [32]. Under this condition, the average electric field in the channel depends on both the inversion and depletion charge [33]. However, in the case of our hybrid MOS-HEMT, which operates in accumulation mode, i.e., the channel is formed on the recessed n-type GaN under the application of a positive bias. Hence, to correctly describe the transport in this structure, the definition of the electric field must be modified. In particular, according to the Gauss's law the effective electric field in the semiconductor as a function of the gate bias is:

$$E_\perp=\frac{V_G-V_{th}}{t_{ox}}\times\frac{\varepsilon_{SiO_2}}{\varepsilon_{GaN}} \quad (5)$$

where V_G is the gate bias, V_{th} is the threshold voltage, t_{ox} is the insulator thickness, and ε_{SiO2} and ε_{GaN} are the insulator and semiconductor relative permittivity, respectively.

For our calculation, we used the following experimental values ε_{SiO2} = 3.9, ε_{GaN} = 9, t_{ox}=50 nm, and V_{th} = +0.7V.

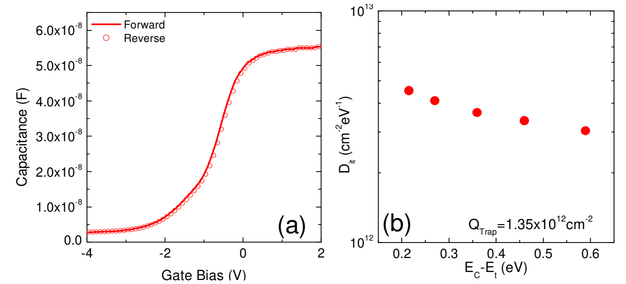

Fig. 3. (a) C-V measurements collected at 1MHz sweeping the bias from depletion to accumulation (forward) and backward (reverse). (b) D_{it} as a function of the energy position E_C-E_t. The density of the trapped charges Q_{trap} (the integral of the interface states) at the SiO_2/GaN interface is estimated to be $1.35\times10^{12}cm^{-2}$

C. *Coulomb Scattering*

Due to the presence of charges trapped at the SiO_2/GaN interface, the free carriers moving in the channel of the hybrid MOS-HEMT are subjected to Coulomb scattering. As mentioned, the hybrid MOS-HEMT operates in accumulation mode. Thus, the amount of the free carriers moving in the channel is the accumulation charge Q_{acc}. The accumulation charge is proportional to the accumulation capacitance C_{ox} and the gate bias V_G, i.e., $Q_{acc}(V_G)=C_{ox}(V_G-V_{th})$. According to the Gauss's law (using Eq. 5), Q_{acc} can be expressed in terms of the effective electric field in the GaN substrate: $Q_{acc}(E_\perp)=E_\perp\varepsilon_0\varepsilon_{GaN}$. Following this assumption, an analogy with the MOSFET mobility model can be done. In particular,

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in accumulation condition it can be assumed that the interface trapped charges (Q_{trap}) induce a screening effect on the free carriers (Q_{acc}) in the channel. Hence, the Coulomb mobility term can be written as :

TABLE I
LIST OF THE PARAMETERS USED IN EQS. 3, 4, 6 AND 8

Parameter	Value	Reference [a]
N_{REF}	3×10^{17} cm^{-3}	31
μ_{max}	1600 cm^{2}V^{-1}s^{-1}	31
μ_{min}	100 cm^{2}V^{-1}s^{-1}	31
β_1	3	31
γ	4.4	31
λ_1	0.7	31
B	1×10^6 cm/s	22
C	3.26×10^6 Kcm/s(V/cm)$^{-2/3}$	22
α_1	0.0284	22
α	1	22
β	1	22
N	0.2336 cm^2/(VsK)$^{-1}$	22
Q_{Trap}	1.35×10^{12} cm^{-2}	This work
l_C	20 nm	This work
σ	0.152 nm	This work
$m_\perp m_\parallel$	$5\times10^{-5}\times m_0^2$ kg^2	This work

$$\mu_C(T;E_\perp)=NT^{\alpha}\frac{Q_{acc}(E_\perp)^{\beta}}{Q_{trap}} \quad (6)$$

where the parameters (N, $\alpha=\beta=1$) have been earlier obtained experimentally for GaN MOSFETs in Ref. [23].

In order to determine the density of the trapped charges Q_{trap} at the SiO_2/GaN interface in Eq. (6), frequency dependent C-V measurements have been carried out on MOS capacitors applying the conductance method [34]. The C-V curves acquired at 1MHz, sweeping the bias from depletion to accumulation and backward, are shown in Fig. 3a. The experimental flat-band voltage was V_{FB}=-0.1V. As can be seen, no hysteresis occurs during the cyclic sweeps. Fig. 4b shows the energy distribution of the interface state density D_{it} at the SiO_2/GaN interface, i.e., in the channel region of the hybrid MOS-HEMT. As can be seen, the value of the interface state density D_{it} close to the conduction band edge (at E_C-E_{it}=0.2eV) is 4.5×10^{12} cm^{-2} eV^{-1} and it decreases moving deeper inside the gap. The value of Q_{trap} has been determined by integrating the D_{it} distribution depicted in Fig. 3b, leading to a value of Q_{trap} =1.35×10^{12}cm^{-2} (see Table I).

In the temperature range explored in this paper, both Q_{trap} Q_{acc} are assumed to be constant.

D. Surface Roughness Scattering

The surface roughness is another physical parameter that influences the MOSFET channel mobility and has been widely debated in literature. In Si MOSFETs, Matsumoto and Uemura [35] proposed a compact expression to describe the surface roughness contribution, i.e., $\mu_{SR}=\delta/E_\perp^{\xi}$, where $E_\perp$ is the perpendicular electric field, and δ and ξ are fitting parameters. Different values of the exponent ξ were reported: ξ=2 is valid only for electrons in Silicon (100) face n-MOSFETs fabricated with thermal gate oxide: lower ξ values have been reported for Si MOSFETs with a nitrided gate oxide; larger ξ up to 3.5 were given for rough Si–SiO_2 interfaces. However, a clear correlation of these fitting parameters with the morphology of the interface was not reported.

Based on numerical calculations of the surface-roughness-limited mobility, Mazzoni et al. [36] demonstrated a correlation between the fitting parameters in the roughness mobility term and the interface quality. In particular, by modifying the model of Matsumoto and Uemura, the dependence of the roughness mobility term on the surface quality and temperature was explicitly given in the relation:

$$\mu_{SR}(T;E_\perp)=\frac{A\left(l_C\,\sigma\right)^{-2}}{(E_\perp/E_0)^{\xi}}\left(1-\frac{T}{T_0}\right) \quad (7)$$

where l_C is the surface correlation length, σ is the surface roughness, and A, T_0, E_0 are fitting parameters depending on the doping of the semiconductor material. However, it has to be emphasized that the two parameters correlated with the surface physical properties (i.e., l_C and σ) were considered as fitting parameters and not directly measured.

More recently, *Zeng et al.* [28] presented a model to study the SiO_2/4H-SiC interface mobility, describing the surface roughness mobility term as:

$$\mu_{SR}(T;E_\perp)=\frac{9h}{8\pi E_\perp}\frac{l_C}{\sigma^2}\left(\frac{\pi}{m_\perp m_\parallel}\right)^{1/2} \quad (8)$$

where $m_\perp m_\parallel$ is the product of the electron effective masses along the electric field direction and the channel direction, l_C is the correlation length, σ is the surface roughness and h is the Plank's constant.

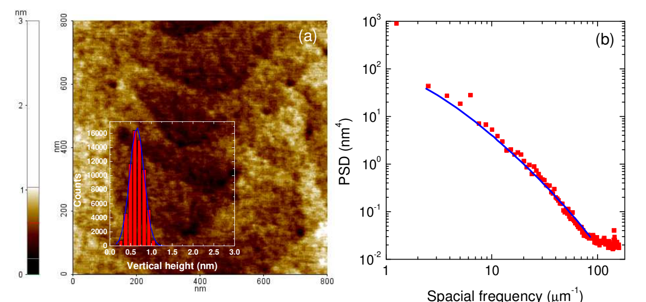

Fig. 4. (a) AFM of the GaN surface after the AlGaN removal. In the inset: the height distribution in the Z direction (orthogonal to the GaN surface) with its Gaussian. (b) 2D Power Spectral Density (PSD) as a function of the spatial frequency of the AFM image and its fit (continuous line) using Eq. 9.

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Also in this case, although the parameters l_C and σ are correlated to the physical properties of the insulator/semiconductor interface, they were considered as fitting parameters. Moreover, one of the assumption was that the high surface disorder of 4H-SiC is a crippling obstacle for carrier transport along the surface [28].

Hence, since in terms of surface roughness values the SiO_2/GaN interface is similar to the SiO_2/SiC, i.e, both are not atomically flat like the SiO_2/Si interface, we used the expression in Eq. 8 to describe the surface roughness mobility in our GaN system.

However, in the present work, l_C and σ were not just considered as fitting parameters but they have been experimentally determined by a nanoscale surface analysis, carried out by AFM.

Fig.4a shows the 800×800nm^2 topography collected with the AFM on the GaN surface after the complete removal of the AlGaN layer. The inset reports the histogram of the heights distribution in the Z-direction (the direction orthogonal to the AFM image XY plane i.e., orthogonal to the GaN surface in the channel region). As can be seen, the experimental heights distribution is well fitted by a Gaussian law, with a correlation index R=0.995. According to C.A. Mack [37], if the 2D topography heights distribution is Gaussian, the 2D Power Spectral Density (PSD) as a function of the spatial frequency f can be analytically described by the following equation:

$$PSD(f) = \pi\sigma^2 l_C^2 e^{-(\pi\, l_C f)^2} \qquad (9)$$

where σ is the standard deviation of the distribution or the root mean square roughness (RMS), and l_C is the correlation length.

Hence, the experimental PSD can be extracted from the AFM image, as the Fourier Transform decomposition of the Z(x,y) heights surface profile into its spatial wavelengths .

Clearly, Eq. 9 contains the two important parameters that enters also in the expression of surface roughness mobility μ_{SR} given in Eq. 8. Hence, using AFM it is possible to experimentally determine the values of σ and l_C:

The PSD determined from the AFM image acquired on the GaN surface in the channel region of the HEMT is reported in Fig. 4b. The experimental PSD data could be fitted using Eq. 9, determining the values of the surface roughness (RMS=σ=0.152 nm) and of the correlation length (l_C=20 nm). As it will be shown in the following section, these values have been used to determine the surface roughness limited mobility contribution and describe the experimental temperature dependence of the mobility.

It has to be mentioned that the surface roughness value was uniform across the 6” wafer, i.e., with values <0.48 nm when acquired on AFM scan areas of 5×5µm^2.

E. *Temperature dependence of the channel mobility*

Fig. 5 reports the maxima of the mobility (peak mobility values) as a function of temperature, extracted from Fig. 2. As can be seen, the experimental peak mobility values decreases with increasing the measurement temperature. The same figure also reports the bulk, acoustic phonon, surface roughness, and Coulomb scattering components (obtained from Eqs. 3, 4, 6 and 8) and the total mobility calculated using the Matthiesen’s rule (Eq. 2). The single mobility components were obtained using the experimental results and the literature data reported in Table I. In particular, the experimental data points in Fig. 5 were matched considering the $m_\perp\, m_\parallel$ coefficient as a unique fitting parameter in surface roughness term in Eq. 8. A good agreement between experimental data and the calculations was obtained for $m_\perp\, m_\parallel = 5\times 10^{-5} \times m_0^2$, m_0 is the free electron mass.

As can be deduced from the data reported in Fig. 5, the main limiting factors for the mobility are the surface roughness (μ_{SR}), the acoustic-phonon (μ_{AC}) and the Coulomb scattering (μ_C) contributions. In fact, due to the larger values of μ_B, ranging from 1600 cm^{2}V^{-1}s^{-1} at room temperature to

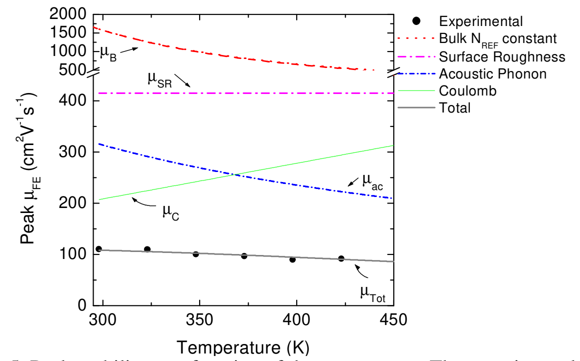

Fig. 5. Peak mobility as a function of the temperature. The experimental data points are compared with the fit (μ_{TOT}) obtained considering the different contributions in the Matthiesen’s rule (μ_B, μ_{SR}, μ_{AC} and μ_C).

about 500 cm^{2}V^{-1}s^{-1} at 450K, it can be assumed that this term has a negligible effect on the total mobility.

F. *Practical implications on the devices performances*

Basing on the above results, some practical implications on the performances of hybrid MOS-HEMTs can be discussed. In fact, the optimization of the device characteristics passes also through the improvement of the morphological and electrical properties of the dielectric/GaN interface in the recessed region. Considering that in our case the roughness of the recessed GaN surface was 0.15 nm, i.e., a value comparable with that of an un-treated surface, the SiO_2/GaN interface states density D_{it} is a crucial parameter that must be controlled in order to improve the device behavior.

Assuming to be able to optimize the interface processing through the reduction of the interface trapped charge Q_{trap}, an improvement of the channel mobility is expected, as can be clearly visualized in the mobility calculations reported in Fig. 5 as a function of the electrical field $E_\perp$. In this figure, the open symbols are the experimental data. As can be seen, a one order

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of magnitude reduction of the interface trap density Q_{trap}, i.e., from the real value of 1.35×10^{12}cm^{-2} (continuous line) down to 1×10^{11}cm^{-2} (dashed line), would lead to an increase of the peak mobility from 110 to 221 cm^{2}V^{-1}s^{-1} at room temperature. It is worth noting that the influence of Coulomb scattering is reduced by decreasing the Q_{trap} (see Eq. 6) and, hence, the peak mobility occurs at a lower electric field value.

To quantify benefit on the device performances, the

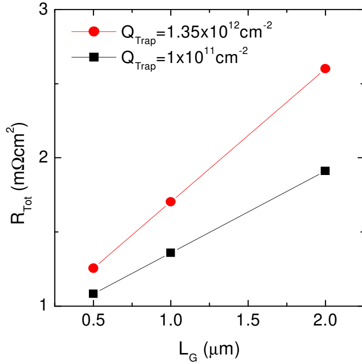

Fig. 7. Total specific on-resistance calculated for different channel lengths .

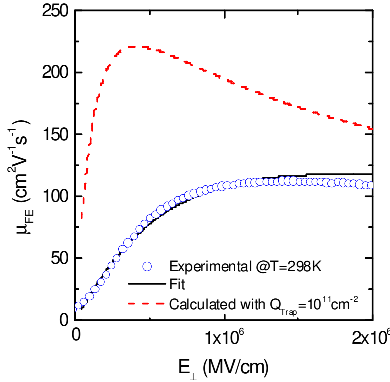

Fig. 6. Experimental (open symbols) and fitted values (black line) of the field effect mobility μ_{FE} as a function of the orthogonal electric field E⊥, at 298K. The calculated curve assuming a reduction of the interface trap density down to 10^{11}cm^{-2} is also reported (dashed line).

reduction of the on-resistance (R_{on}) in MOS-HEMT structures has been calculated for the two values of Q_{trap} and different gate lengths This comparison has been done for an electric field of $E_{\perp}$= 1.5MV/cm (Q_{trap} constrant) the reduction of Q_{trap} results into an increase of the channel mobility from 110 to 173 cm^{2}V^{-1}s^{-1} at room temperature. Consequently, a reduction of the sheet resistance below the gate from $R_{sh,exp}$=7.3kΩ/sq to $R_{sh,lowQtrap}$=4.65kΩ/sq can be estimated.

The total specific on-resistance (R_{on}) of MOS-HEMTs has been calculated for different channel length values from 0.5 up to 2 µm, and is shown in Fig. 8.

In our R_{on} calculation, we assumed a source-drain distance of 13 µm, which is a realistic value for fabricating hybrid MOS-HEMT with a breakdown voltage of 600V onto a 2.3 µm thick GaN buffer [38]. Moreover, reasonable values of the contact resistance (R_C=0.5Ωmm) and of the sheet resistance of the AlGaN/GaN heterostructure ($R_{sh,2DEG}$=400Ω/sq) were considered. As can be seen in Fig. 7, the reduction of the Q_{trap}, induces a 35% reduction of R_{on} for a hybrid MOS-HEMT with L_G=2 µm. This advantage remains significant (14% reduction of R_{on}) even for shorter gate length (L_G=0.5 µm).

IV. Conclusion

In this paper, the channel mobility in GaN MOS-HEMTs has been studied, considering the different contributions to the mobility, adapted to the specific case of the MOS-HEMT operating in accumulation. A combination of electrical measurements on transistors and capacitors, and nanoscale surface analysis on the recessed GaN surfaces, allowed to derive meaningful physical parameters for this model. The temperature dependence of the peak mobility suggested that main limiting factors to the carrier flow in the channel are phonon and Coulomb scattering effects. The implications in practical devices have been discussed, considering the possible R_{ON} reduction that can be obtained by improving the SiO_2/GaN interface. In particular, it has been shown that a reduction of one order of magnitude of the interface states density can lead to a R_{on} reduction ranging between 14 and 35% for 600V MOS-HEMT devices. The results are important to understand the mobility behavior on the MOS-HEMT channel and, ultimately, to optimize the devices performances.

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