Effects of annealing treatments on the properties of Al/Ti/p-GaN interfaces for normally-off p-GaN HEMTs

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Abstract— **This paper reports on the behavior of Al/Ti/p-GaN interfaces as gate contacts for p-GaN/AlGaN/GaN normally-off HEMTs, highlighting the impact of the thermal budget on the metal gate on the device characteristics. In fact, while the devices subjected to an annealing at 800 °C show a considerable high leakage current, those with non-annealed Al/Ti gate contacts exhibit a normally-off behavior, with a pinch-off voltage V_{po}= +1.1 V and a on/off current ratio of 3×10^8. Temperature dependent electrical measurements on "back-to-back" Schottky diodes allowed to determine a Schottky barrier height Φ_B of 2.08 eV and 1.60 eV, for the non-annealed and 800 °C annealed gate contacts, respectively. Hence, the increase of the leakage current observed upon annealing at 800 °C was attributed to the lowering of the Schottky barrier height Φ_B of the metal gate. The interfacial structural characterization explained the barrier lowering induced by the annealing. This scenario was discussed through the simulated band diagram of the heterostructures, considering the experimental values of Φ_B. These results provide useful information for the device makers to optimize the fabrication flow of normally-off HEMTs with p-GaN gate.**

Index Terms — **AlGaN/GaN heterostructures, p-GaN, High Electron Mobility Transistors (HEMTs), Enhancement mode operation, Schottky barrier**

I. Introduction

NOWADAYS, wide band gap semiconductor materials are considered as the best candidates for the next generation of power electronic devices with a high energy efficiency [1,2,3]. In particular Gallium Nitride (GaN) possesses excellent physical properties, such as a high critical electric field and a high saturation velocity [4], allowing to fabricate devices with a low specific on-resistance, a high breakdown voltage, and a high operation switching frequency. Moreover, thanks to the presence of a strong built-in polarization, the combination of GaN and with its related $Al_xGa_{1-x}N$ alloys offers the possibility to fabricate High Electron Mobility Transistors (HEMTs) [5]. Due to the presence of a two-dimensional electron gas (2DEG) at the AlGaN/GaN interface, these devices have inherently a normally-on behavior, i.e., in their standard configuration they are piloted by the application of a negative bias to a Schottky gate contact to modulate the sheet carrier density in the 2DEG channel. However, in many practical applications, normally-off transistors are desired to provide adequate safety conditions for the equipment and for the users [6,7]. For that reason, understanding the physics to develop a reliable process for normally-off HEMTs represents a big challenge for the current GaN-based technology.

In the last years, several technological solutions have been proposed to fabricate normally-off GaN-based HEMTs, e.g., the use of fluorine-based plasma treatments below the gate [8], the use of a piezo-neutralization layer [9], the non-polar a-plane channel [10], the metal–oxide–semiconductor field-effect transistor [11] and the "recessed-gate" structure [12]. Among them, the combination of a recessed MOS channel region within a standard AlGaN/GaN HEMT layout (referred as hybrid MOS-HEMT) offers the possibility to achieve a stable positive threshold voltage V_{th} [13]. In this context, oxidations at high temperatures (800-900 °C) have been also investigated as possible treatments to positively shift the V_{th} and control the 2DEG in AlGaN/GaN heterostructures [14,15].

Another promising approach consists in the use of a p-type GaN or AlGaN gate on the AlGaN/GaN heterostructure to deplete the 2DEG [16,17,18,19]. The big advantage of this solution is the possibility to obtain a high positive threshold voltage V_{th} (up to 3 V) [18]. In fact, with its large band gap (3.4 eV) and the Fermi level (E_F) close to the valence band (E_V), a p-GaN cap layer onto an AlGaN/GaN heterostructure is able to significantly lift up the potential at the channel, allowing the depletion of the 2DEG and, hence, leading to normally-off operation. However, the optimization of the p-GaN gate HEMT technology passes through the comprehension of several physical issues related to the interfaces with the p-GaN layer. As an example, while the role of the metal/semiconductor barrier height on the modulation of the 2DEG density has been widely discussed in conventional AlGaN/GaN heterostructures [20,21,22,23], the importance of the metal gate on p-GaN gate HEMTs still deserves further investigation. In fact, only recent papers started to discuss the influence of the metal work-function Φ_m on the devices characteristics, reporting that a high metal/p-GaN Schottky barrier height can reduce the gate leakage current and increase the threshold voltage in p-GaN/AlGaN/GaN HEMTs [18,24]. However, it is well known that, rather than on the metal work function Φ_m only, the Schottky barrier height value depends on several experimental

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conditions related to the device fabrication (metal deposition technique, surface preparation, annealing conditions, semiconductor surface defects, etc.). In this sense, in spite of the good performances of the reported devices [16,17,18], the properties of the most common metal/p-GaN gate barriers require additional studies.

In this paper, we have investigated the properties of metal/p-GaN interfaces, with a special focus on the effects of the annealing treatments on the electrical and structural properties of Ti/Al layers used as gate contacts for p-GaN/AlGaN/GaN HEMTs. In particular, the device characteristics strongly depend on the thermal budget experienced by the metal gate. The increase of the device leakage current observed with increasing annealing temperature has been attributed to a lowering of the Al/Ti/p-GaN Schottky barrier height, monitored by a temperature dependent electrical analysis. The structural modifications occurring at the interface explained this behavior. The scenario was further discussed through the simulated band diagram of the heterostructures with the different experimental barrier height values. The results presented in this work provide useful information to optimize the fabrication flow of normally-off p-GaN gate HEMTs.

II. Device Fabrication

HEMTs have been fabricated on p-GaN/AlGaN/GaN heterostructures grown on Si-substrates. The heterostructure consisted of a 10 nm thick $Al_{0.26}Ga_{0.74}N$ barrier layer grown onto a 1 µm unintentionally doped (u.i.d.) GaN buffer. A Mg-doped p-GaN layer with a doping concentration of 3×10^{19} cm^{-3} and a thickness of 50 nm was grown on the top of the AlGaN/GaN template. To define the p-GaN gate regions, a Cl-based plasma etch was carried out using a Roth & Rau Microsys 400 ICP equipment. Ohmic contacts were formed by Ti/Al/Ni/Au (15/200/50/50 nm) annealed at 800 °C in Ar for 60 s [25], while a Ti/Al (30/170 nm) bilayer was used as gate contact onto the p-GaN. In order to get insights into the devices physics and the behavior of the metal gate, two different processing conditions have been compared. In the first case, the Ti/Al gate contact has been fabricated prior to Ohmic contact formation ("gate first" approach, GF). Hence, the Ti/Al gate electrode experienced the thermal budget (800 °C for 60 s) used to achieve Ohmic behavior. In the second case, the Ti/Al gate contact was defined onto the p-GaN regions only after Ohmic contacts formation and annealing ("gate last" approach, GL). Clearly, in this case the metal gate was not subjected to thermal annealing. The fabricated devices were round HEMTs with gate length (L_G) of 20 µm, gate width (W_G) of $2\pi\cdot65$ µm and source-drain distance (d_{SD}) of 40 µm.

In order to study the physical and electrical properties of Al/Ti/p-GaN interfaces (i.e., the gate region), Ti/Al contacts have been fabricated on blanket p-GaN samples following the same procedure adopted for HEMTs devices. In this case, a p-GaN layer with the same doping concentration (3×10^{19} cm^{-3}) and a thickness of 200 nm, grown onto a 1 µm thick u.i.d. GaN layer on Si substrate has been used. On these samples, test patterns for electrical measurements have been fabricated and characterized before and after annealing (400-800 °C for 60 s). All thermal processes have been carried out by a rapid thermal annealing (RTA) Jipelec JetFirst furnace.

Current - Voltage (I-V) measurements were carried out using a Karl Suss Microtec probe station equipped with a HP4156B parameter analyzer. The I-V measurements were performed as a function of the temperature in the range 25-200 °C. Transmission Electron Microscopy (TEM) analysis in cross section, coupled with Energy Filtered Transmission Electron Microscopy (EFTEM), was performed using a 200 kV JEOL 2010 F microscope to monitor the interface structural modifications upon annealing. Finally, the band diagram of the p-GaN/AlGaN/GaN heterostructure have been simulated by commercial SILVACO simulator, using the experimental parameters determined by the experimental I-V measurements [26].

III. Results And Discussion

The I-V characteristics of the HEMTs devices fabricated with the "gate first" (GF) processes, i.e., with the Ti/Al gate contact annealed at 800°C, are shown in Fig. 1(a). Clearly, the I-V characteristics of these devices are affected by a high leakage current, which can be associated to the gate contact. In fact, at low V_{DS} values a negative drain current is measured, and it increases with increasing the gate voltage (V_G). Fig. 1(b) reports the drain current I_{DS}, the gate current I_G and the g_m of the devices as function of the gate bias V_G for a drain bias V_{DS}= +10 V. Here, due to the high leakage of the gate, a current is measured at the drain even when the channel should be depleted. For that reason a normally-on behavior is observed with a negative shift of the pinch-off voltage (V_{po}=-1.0V).

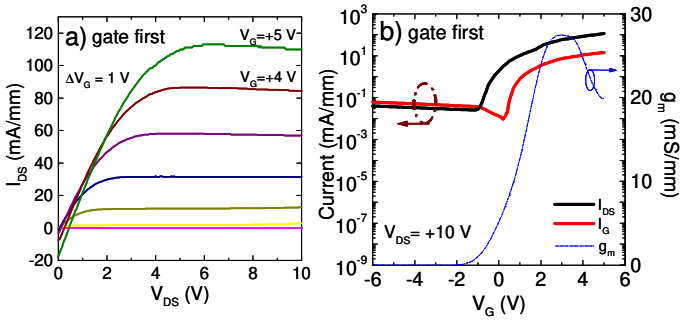

Fig. 1: I-V characteristics of the p-GaN/AlGaN/GaN HEMT devices fabricated using a "gate first" process, i.e., with the Ti/Al gate annealed at 800 °C (a). Drain current (I_{DS}), gate current (I_G) and g_m acquired at V_{DS}= +10 V on the same devices (b).

The I-V characteristics of the p-GaN HEMTs fabricated with the "gate last" (GL) approach, i.e., with the "non-annealed" Ti/Al gate contact, are shown in Fig. 2(a). Evidently, in this case the leakage current is significantly

lower than that observed in the GF devices. The drain current I_{DS}, the gate current I_G and the g_m of the GL devices are shown in Fig. 2(b) as function of the gate bias V_G for a V_{DS}= +10 V. The GL devices show a clear normally-off behavior, as can be seen from the positive pinch-off bias V_{po}= +1.1 V, with a on/off ratio of 3×10^8. Moreover, the I_D-V_{GS} and the I_G-V_{GS} curves shown in Fig. 2 exhibit the presence of a kink at a gate bias of about V_G=+5 V. This behavior can be associated to the occurrence of holes injection from the p-GaN into the channel, as explained by Uemoto et al. [16] in similar devices.

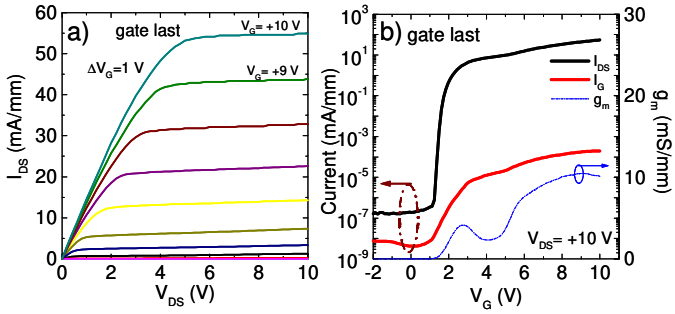

Fig. 2: I-V characteristics of the p-GaN/AlGaN/GaN HEMT devices fabricated using a "gate last" process, i.e., with a non-annealed Ti/Al gate (a). Drain current (I_{DS}), gate current (I_G) and g_m acquired at V_{DS}=+10 V on the same devices (b).

The trade-off between the saturation drain current (I_{Dmax}) and on-state gate leakage ($I_{G\text{-}ON}$) is graphically reported in Fig. 3. In particular, the figure reports the ratios $I_D$maxGL/$I_D$maxGF and $I_{G\text{-}ON}$GL/$I_{G\text{-}ON}$GL as a function of V_{GS}-V_{TH}, being V_{TH} the threshold voltage determined by the transcharacteristics in the saturation region (V_{TH}GL=1.5V and V_{TH}GF=-0.6V. Even if a lower saturation drain current is measured in the GL devices, a reduction of the gate leakage current $I_{G\text{-}ON}$ of about six orders of magnitude with respect to the GF devices is obtained in this case. Clearly, as can be seen in Fig. 1, a much more limited gate voltage swing is possible in the GF device, due to the occurrence of a high leakage current already at V_{GS}=3V. On the other hand, the lower leakage in the GL HEMT can be a considerable advantage, in terms of device reliability under long term operation. Additionally, a lower I_G leads also to a decrease of the energy consumption to drive the device.

As reported in Refs. [19] and [24] the saturation drain current in p-GaN gate HEMTs can be affected by different factors, like the barrier height of the metal gate (which has an impact on the 2DEG below p-GaN) or inhomogeneities of the selective plasma etch process of the p-GaN. In our case, both factors contribute to the different experimental drain current in the two cases. In fact, as will be shown in the following part of the paper, a larger barrier height was measured in the GL device. Moreover, TEM analysis (not reported here) revealed the presence of an inhomogeneous residual p-GaN layer on the surface access regions. Such residuals are related to the critical control of our p-GaN dry etch process. These experimental evidences justify our results.

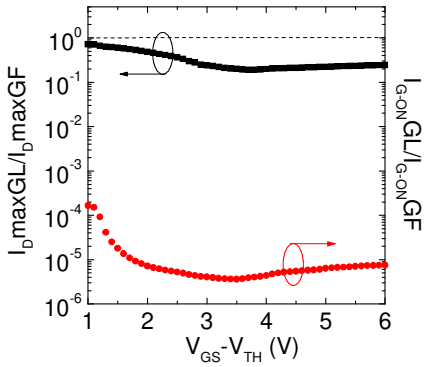

Fig. 3: The trade-off between the saturation drain current ($I_D$max) and the on-state gate leakage ($I_{G\text{-}ON}$). The figure reports the ratios $I_D$maxGL/$I_D$maxGF and $I_{G\text{-}ON}$GL/$I_{G\text{-}ON}$GL as function of the V_{GS}-V_{TH}.

To explain the behavior of the metal/p-GaN interface upon annealing treatment, Ti/Al Schottky contacts have been deposited on blanket p-GaN samples, as described in the experimental session. Then, the modifications of the metal/p-GaN interface with the annealing treatments have been first investigated by electrical measurement. For this purpose, appropriate test patterns, i.e., "back-to-back" Schottky contacts at a distance of 10 μm, have been fabricated and characterized before and after annealing of the sample at 400 °C and 800 °C. This test pattern, schematically depicted in the inset of Fig. 4, consists in the series of two Schottky contacts, one in forward and the other in reverse bias [27]. In this configuration, the total resistance (R_T) is given by R_T=R_1+R_2+R_B, where R_1 and R_2 are the resistances of the two diodes and R_B is the resistance of the p-GaN layer. At moderate bias (e.g., V < 0.8 V), the small reverse current, limited by the high interface resistance (R_1 or R_2), is the dominant contribution at the p-GaN/Ti/Al interface [27,28,29]. A further increase of the bias leads to a rapid increase of the reverse current, i.e., a strong decrease of the resistance related to reverse biased diode (R_1 or R_2). In this condition, the contribution of the metal/p-GaN interface becomes smaller and the total resistance can be approximated to $R_T \approx R_B$. This value depends on the p-GaN resistivity and can be expressed as R_B=ρ×(d/S), where d is the distance between the metal contacts, S the is the cross-sectional area of p-GaN between the contact and ρ is the resistivity of p-GaN. In our "back-to-back" diodes, the resistivity of the p-GaN estimated from the slope of the I-V curves at high voltage was ρ=4 Ω·cm. This value is in very good agreement with the one extracted independently using Van-der-Paw structures.

The I-V measurements carried out on the back-to-back diodes in the bias range 0-3 V , reported in Fig. 4, show an increase of the current with increasing annealing temperature. Based on this evidence, it can be deduced that the annealing treatments induce significant modifications to the metal/p-GaN barrier.

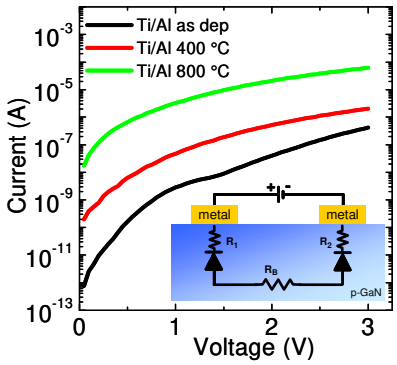

Fig. 4: I-V characteristics acquired in "back-to-back" p-GaN/Ti/Al Schottky contacts, for the as deposited sample and for the samples annealed at 400 °C and 800 °C. The inset shows the equivalent circuit of the investigated "back-to-back" Schottky contacts.

To get further insights into the transport properties at the Schottky interfaces, the temperature dependence of the current-voltage (I-V) characteristics have been studied for these systems. In Fig. 4, the current measured at V= +0.2 V in the "back-to-back" p-GaN/Ti/Al Schottky contacts is reported as function of the measurement temperature, for the "as deposited" (non-annealed) sample and for the samples annealed at 400 °C and 800 °C. Evidently, in all three cases the current increases with increasing measurement temperature. Typically, the ratio qE_{00}/kT gives an indication on the mechanism dominating the current transport [30]. In our case, considering a Mg doping of 3×10^{19} cm^{-2}, it is possible to estimate a qE_{00}/kT ratio in the range 1.47-0.84 in the examined temperature range. This latter suggests that the Thermionic Field Emission (TFE) is the dominant mechanism of current transport. On the other hand, Fukushima et al. [31] reported that the current transport is dominated by the Thermionic Emission mechanism for a p-type GaN samples with a lower Mg-concentration (1.3×10^{18} cm^{-2}).

Hence, the expression of the TFE reverse current was used to fit our experimental data [28,32,33,34]:

$$I_S = \frac{A_c A^* T \sqrt{\pi E_{00}}}{k} \cdot \sqrt{q(V - V_n) + \frac{q\Phi_B}{\cosh^2\left(\frac{E_{00}}{kT}\right)}} \cdot \exp\left(-\frac{q\Phi_B}{E_{00}\coth\left(\frac{E_{00}}{kT}\right)}\right) \quad (1)$$

$$I_{TFE} = I_S \cdot \exp\left[\frac{qV}{kT} - \frac{qV}{E_{00}\coth\left(\frac{E_{00}}{kT}\right)}\right] \quad (2)$$

with

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right) \quad \text{and} \quad E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_A}{m^*\varepsilon}} \quad (3)$$

and where V is the applied voltage, A_c is the contact area, A^* is the Richardson constant, q is the elementary charge, k is the Boltzmann constant, h is the Plank constant and T is the absolute temperature. In the above expressions, ε and m^* are respectively the dielectric constant for GaN and the effective mass for holes in GaN. Φ_B and N_A represent the Schottky barrier height of the metal/p-GaN interface and the doping concentration of the semiconductor. In our calculation we used the values of $\varepsilon=8.9\varepsilon_0$, where ε_0 is the permittivity of free space, $A^*=27.9$ A/cm^{2}K^2, and $m^*=0.81m_0$, with m_0 the free electron mass [33].

From the TFE fit of the experimental data, the relevant physical parameters characterizing the Al/Ti/p-GaN/ interface (Φ_B and N_A) have been determined in the three different cases (as deposited, 400 °C and 800 °C).

In particular, in the as deposited sample a Schottky barrier height $\Phi_B = 2.08$ eV has been found. This value is in reasonable agreement with the theoretical one, $\Phi_{Btheor} = E_g - (\Phi_m - \chi) = 2.3$ eV, obtained considering the GaN energy gap ($E_g = 3.4$ eV), the Ti metal work function ($\Phi_m = 4.3$ eV) and the GaN electron affinity ($\chi = 3.2$ eV). Moreover it is also consistent with other experimental values reported in literature for Ti/p-GaN interface [32,35]. On the other hand, by increasing the annealing temperature, a lowering of Φ_B occurs, down to 1.87 eV and 1.60 eV for the sample annealed at 400 °C and 800 °C, respectively.

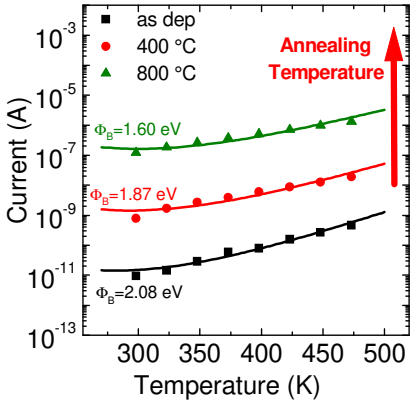

Fig. 5: Temperature dependence of the current measured at V= +0.2 V in "back-to-back" p-GaN/Ti/Al Schottky contacts, for the as deposited and for the samples annealed at 400 °C and 800 °C.

From our analysis, the same doping level $N_A \approx 5\times10^{19}$ cm^{-3} has been determined in all three conditions, thus indicating that the thermal processes did not induce significant modifications of the p-GaN layer. However, it is worth noting that the value of the doping concentration determined by the fit is a factor of 1.67 larger than the nominal acceptor concentration ($N_A = 3\times10^{19}$ cm^{-3}). As often reported in literature, this discrepancy can be attributed to the large amount of defect states near the surface of p-GaN materials

[36,37,38,39]. In particular, as already reported in Ref. [36,37], an increase of acceptor-like deep level defects (DLDs) can occur in p-GaN layers with a comparable Mg-doping. Capture and emission from these defects have been usually correlated with an increase of the leakage current at the interface [38]. Moreover, in the presence of these defects, the depletion layer width in the near-surface p-GaN is reduced. Consequently, the probability of TFE through the barrier increases (i.e., a higher E_{00}), thus resulting into a higher calculated N_A [39].

To give a physical explanation to the modification of the Schottky barrier height revealed by the temperature dependent I-V characteristics after the different annealing treatments, a cross section TEM analysis of the annealed interface has been performed. Fig. 6(a) shows the cross section TEM image of the p-GaN/Ti/Al structure annealed at 800 °C. The Energy Filtered Transmission Electron Microscopy (EFTEM) chemical maps of Al and Ti are also shown in Fig. 6(b) and Fig. 6(c), respectively. During the annealing treatment, a part of the Al was consumed, reacting with Ti to form an $TiAl_3$ alloy. On the other hand, part of the unreacted Al diffused towards the interface. Hence, an inhomogeneous composition of the metal/p-GaN interface is observed, i.e., with the presence of both Al and $TiAl_3$ in contact with the p-GaN.

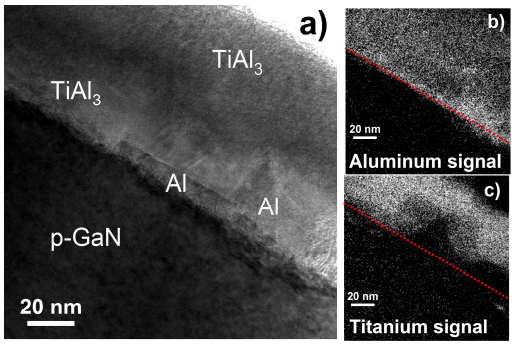

Fig. 6: Cross section TEM micrographs of the p-GaN/Ti/Al interface annealed at 800 °C (a). Chemical maps acquired by EFTEM for Aluminum (b) and Titanium (c). The red dashed lines indicates the metal/p-GaN interface.

Based on this result, the reduction of the Schottky barrier height observed with increasing annealing temperature, can be associated to the presence of different phases at the interface with the p-GaN, plausibly with a different work function. A similar behavior has been already observed also on Ti/Al-based contacts to p-type silicon carbide [40,41]. Clearly, the reduction of the Schottky barrier height enhances the tunnelling of the holes through the barrier. Hence, the high leakage current detected in the GF devices (annealed at 800 °C) can be explained by a lowered barrier height at the metal/p-GaN contact. Similarly, Lee *et al.* [24] showed different electrical characteristics of p-GaN gate HEMTs using different metal gates, but a clear correlation with the barrier height was not reported in that work.

To better discuss this scenario, the band diagram of the fabricated p-GaN/AlGaN/GaN heterostructures has been simulated at the gate bias of V_{GS}= +4 V, both for the as deposited sample and for the sample annealed at 800 °C, i.e., using the experimentally determined values of the barrier height (2.08 eV and 1.60 eV, respectively). The simulated band structures are reported in Fig. 7(a) and Fig. 7(b).

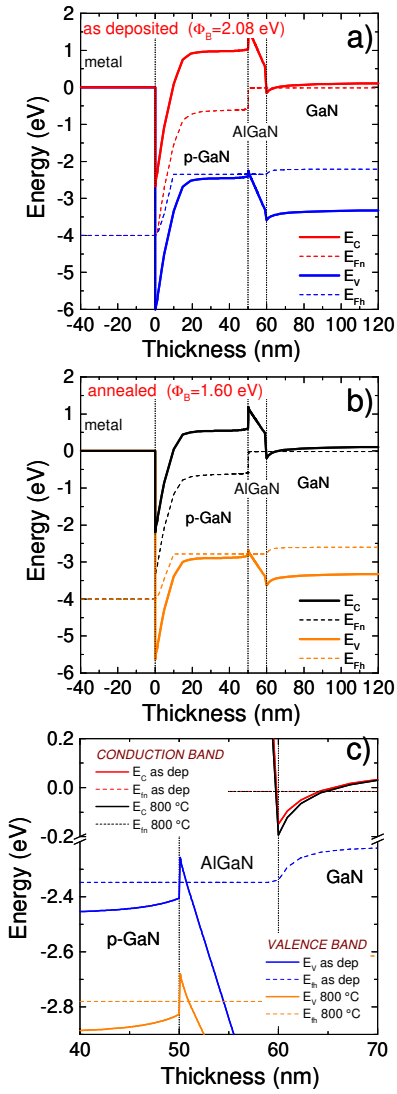

Fig. 7: Simulated band diagram of the p-GaN/AlGaN/GaN heterostructure at a gate bias V_{GS}= +4 V for the as deposited (Φ_B= 2.08 eV) (a) and for the 800 °C annealed (Φ_B= 1.60 eV) Ti/Al gate contact (b). The quasi-Fermi levels for electrons E_{Fn} and holes E_{Fh} are also shown. A magnification of the conduction band at the AlGaN/GaN interface and of the valence band at the p-GaN/AlGaN interface (c).

Two different junctions characterize these heterostructure, i.e., the metal/p-GaN interface and the p-GaN/AlGaN interface. Clearly, in both devices, at a gate bias of V_{GS}=+4 V the 2DEG quantum well is located below the Fermi level. Moreover, at the same V_{GS}=+4 V, a higher sheet carrier density has been obtained (5.69×10^{12} cm^{-2}) for the annealed device with respect to the non-annealed one (4.21×10^{12} cm^{-2}). Accordingly, in case of the device annealed at 800 °C (GF), a lower V_{GS} has to be applied in order to completely deplete the 2DEG, with respect to the as deposited device (GL). The

simulated values of the threshold voltage V_{TH} were +0.7 V and +1.5 V, for the GF and GL devices, respectively. Clearly, in the case of the GL device there is a good agreement between experiment and simulation. On the other hand, a negative threshold voltage is experimentally estimated in the GF sample (V_{TH}GF= -0.6V), due to the high leakage current. Consequently, a discrepancy with respect to the simulated value occurs in this case. Moreover, at a gate bias of V_{GS}= +4 V, the holes that are close to the p-GaN surface (below the gate electrode) are depleted and tend to accumulate in the other side, i.e., at the p-GaN/AlGaN interface. Hence, under a positive gate bias, holes can be injected from the p-GaN towards the AlGaN layer more easily in the sample with a lower barrier (GF , annealed 800 °C) with respect to the one with a higher barrier (GL, non-annealed).

The presence of a higher holes concentration in the sample with a lower barrier can be understood from the energy difference between the valence band and the quasi-Fermi level for holes, at the p-GaN/AlGaN interface, in Fig. 7(c). Clearly, the presence of the two junctions (metal/p-GaN and p-GaN/AlGaN) determines the behavior of the gate current under positive and negative bias. In fact, as recently pointed out by Wu et al. [42], under a positive gate bias, the accumulation of holes at the p-GaN/AlGaN interface is accompanied by the emission of 2DEG electrons over the AlGaN barrier that are driven through the p-GaN layer towards the gate electrode. Obviously, a higher metal/p-GaN Schottky barrier will result into a wider p-GaN depletion region and, hence, into a lower gate current. On the other hand, under negative bias the Fermi level lies below the conduction band, thus corresponding to the 2DEG depletion. Hence, the gate leakage current is determined by the holes driven towards the gate electrode.

IV. Conclusion

In this paper, the electrical and structural behavior of Al/Ti/p-GaN interfaces has been investigated, focusing on the effects of the annealing treatments on the properties of Ti/Al contacts used as gate for normally-off p-GaN/AlGaN/GaN HEMTs.

In particular, a normally-off behavior with a pinch-off bias of V_{po}= +1.1 V and a on/off ratio of 3×10^8 have been obtained in the "gate last" HEMT devices, i.e., where the Ti/Al gate was not subjected to thermal budget. On the other hand, HEMT devices annealed at 800 °C ("gate first") exhibited a significantly higher leakage current.

A combination of temperature dependent current-voltage measurements with structural analyses allowed to explain the device behavior. In fact, the decrease of the Schottky barrier height from 2.08 eV to 1.60 eV upon annealing at 800 °C was ascribed to the structural modification occurring at the interface and explained the increase of the leakage current. This scenario was better described with the help of the simulated band diagram, which explained the increase of the leakage current in terms of the holes injection occurring upon a positive gate bias.

The results presented in this paper can provide useful information for a better comprehension of metal/p-GaN system on heterostructures, to define an optimal fabrication process for normally-off p-GaN gate HEMTs.

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