Envelope Tracking of an RF High Power Amplifier with an 8-level Digitally-Controlled GaN-on-Si Supply Modulator

Corrado Florian, *Member, IEEE*, Tommaso Cappello, *Member, IEEE*, Rudi Paolo Paganelli *Member, IEEE*, Daniel Niessen, *Member, IEEE*, and Fabio Filicori

***Abstract*— This paper presents an envelope tracking (ET) transmitter architecture, based on the combination of a novel 3-bit (N = 3) supply modulator and digital predistortion (DPD). The proposed power converter is based on a direct digital-to-analog conversion architecture that implements the binary-coded sum of N isolated dc voltages, allowing the synthesis of an output waveform with $L = 2^N$ voltage levels, with a binary distribution in the range $\Delta V = V_M - V_O$ (maximum voltage V_M, offset voltage Vo). This solution provides a better voltage resolution $V_S = \Delta V/(2^N-1)$, with respect to typical multilevel switched-sources topologies ($V_S = \Delta V/N$). The improved voltage resolution enables the correction of the residual discretization error in the ET transmitter by means of DPD of the RF signal, without the need of an auxiliary linear envelope amplifier. The proposed ET solution has been tested with an L-band 30-W lateral-diffused MOS (LDMOS) RF high power amplifier (RF HPA) with 1.4- and 10-MHz long-term-evolution (LTE) signals. In these conditions the converter demonstrated 92% and 83% efficiency, respectively, whereas the congregate efficiency of the transmitter are 38.3% and 23.9% at 5.5 W and 1.9 W of average RF output power, respectively. These performances correspond to an improvement of 17.2 and 17.9 points for the power added efficiency of the RF HPA and to 13.4 and 13 points of improvement for the efficiency of the entire transmitter with respect to fixed bias operation.**

***Index Terms* — Envelope Amplifier, Envelope Tracking (ET), GaN technology, multilevel converters, power digital-to-analog converter (power-DAC), supply modulator.**

I. Introduction

Modern wireless communication systems such as third generation (3G), long term evolution (LTE) and worldwide interoperability for microwave access (WiMAX) employ large bandwidth (BW) digital modulated signals (1-20 MHz) with very high peak-to-average power ratio (PAPR) to enhance spectral efficiency and maximize the data rate [1]-[10]. While high PAPR modulations are very effective in terms of data throughput, they are strongly detrimental for the RF amplifier efficiency, compared to constant envelope digital modulation standards (e.g. GSMK, PSK, MSK). Indeed, due to the high PAPR of the modulated signals, the RF high power amplifier (HPA) operates for most of the time at very low efficiency [1], [9]-[15]. Thus, RF HPA efficiency in the order of 10%-25% or less is quite typical for this kind of systems [11], [13], [16], [17]. A common technique to enhance the RF HPA efficiency is Envelope Tracking (ET), which employs a dynamic bias supply that follows a set point (*i.e.* the so called *supply shaping function*) proportional to the input RF signal envelope to maintain the RF HPA operating condition close to a high efficiency regime, which corresponds to a certain level of gain compression [14]. ET is usually used in combination with Digital Pre-Distortion (DPD) to recover the signal linearity [1], [2], [5]-[7], [10]-[12], [15]. The combination of ET and DPD can considerably improve the RF HPA efficiency [1], [2], [6]-[8], [15], while maintaining the required linearity performance.

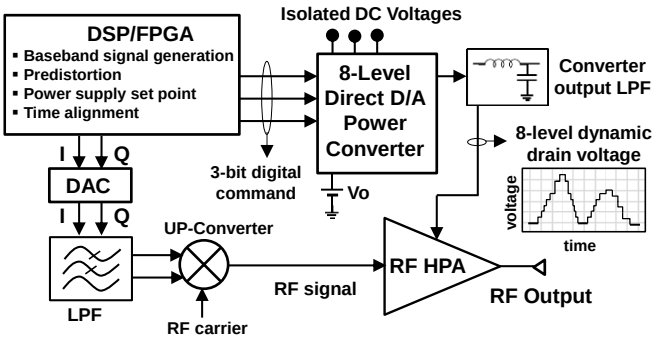

Fig. 1. Architecture of the proposed ET transmitter.

The efficiency of the supply power converter is equally important for overall efficiency of the ET transmitter. Therefore, in ET architectures, the power converter, which, in the case of fixed bias is a conventional high efficient dc-dc switching regulator, must be replaced by an envelope amplifier or supply modulator, with very demanding specifications in terms of bandwidth, linearity and dynamics, and with the highest possible conversion efficiency [14]. Several examples of high-performance envelope amplifiers/supply modulators for ET applications can be found in the literature, aiming at the maximization of bandwidth and efficiency [1]-[9], [11]-[13], [15]-[25]. These designs basically belong to three possible architectures (or a combination of them): 1) Linear-assisted pulse width modulated (PWM) switching converters; 2) multiphase switching converters; and 3) Multilevel converters.

The proposed ET architecture is described in Fig. 1. It is based on a novel multilevel power converter, based on a direct digital-

Corrado Florian, Tommaso Cappello, Daniel Niessen and Fabio Filicori are with the Department of Electrical, Electronic and Information Engineering (DEI) of the University of Bologna, Bologna, 40136, Italy (corrado.florian@unibo.it). Rudi Paolo Paganelli is with the National Research Council, Institute of Electronics, Computer and Telecommunication Engineering (CNR-IEIIT), Bologna, 40136, Italy.

to-analog conversion architecture that implements the binary-coded sum of three isolated dc voltages, allowing the synthesis of an output waveform with eight voltage levels. The circuit is controlled by digital signals coming directly from the transmitter base-band FPGA, without the need for digital-to-analog conversion and envelope detector circuitry and comparators adopted by analog envelope amplifiers for RF transmitters [1].

The proposed converter is different from typical multilevel converters based on commutated-voltage-source architectures as in [9], [13], [16], [19], [40]: while in these solutions the number of output voltage levels L is equal to the number N of the input voltage sources V_N, for the proposed circuit $L=2^N$, due to the capability of its topology and controlling strategy to implement the binary-coded sum of the N input dc voltages, rather than their simple selection. Consequently, the output voltage resolution is improved from $V_S = \Delta V/N$ to $V_S = \Delta V/2^N$-1. With this finer voltage resolution, the residual discretization error in the transmitter RF output signal is reduced and can be compensated by means of DPD of the RF signal, without the need of an auxiliary linear envelope amplifier that is responsible of efficiency degradation in both traditional multilevel [13], [16], [19] and linear assisted switching converter architectures [8], [9], [12], [17], [20], [26], [27], [29], [30].

The proposed power converter is designed exploiting very fast discrete GaN-based power switches [34], embedded in an extremely compact circuit layout, that guarantee low commutation losses, even at high operating frequencies.

This direct digital-to-analog power conversion implemented by the circuit, practically makes the proposed converter a power digital-to-analog converter (DAC), *i.e.* a Power-DAC.

The paper is organized as follows. In Section II, the converter topology, components and working principles are described. Section III covers the circuit design and simulation. In Sections IV and V, characterization measurements of the power converter and of the entire transmitter setup are proposed. Finally, some conclusions are drawn in Section VI.

II. Converter Topology and Technology

The architecture of the proposed converter is described in Fig. 2. This type of structure, referred as *cascaded multicell architecture* [31]-[33], is typically used for high power, very low-frequency applications as in the inverters for photovoltaic systems or high-power machine drives [31]-[33], where bandwidths of a few hundred hertz are targeted.

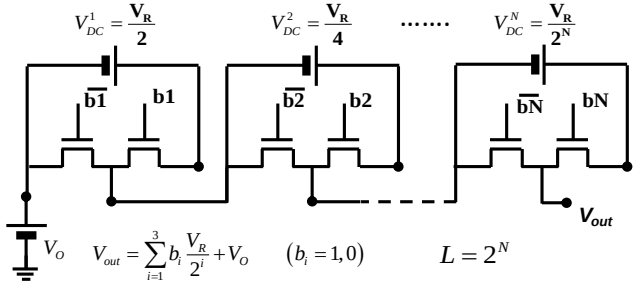

Fig. 2. Binary asymmetric cascaded multilevel structure (plus offset V_O) adopted for the Power-DAC topology.

In this paper this configuration is applied for the first time to a completely different application, targeting lower power levels and bandwidths which are four orders of magnitude higher than its typical applications [31]-[33].

Cascading N half bridge (HB) converters as in Fig. 1, connected to N asymmetric (power of two) isolated voltage sources (*i.e.* dc links, $V_{DC}^i = V_R/2^i$ in Fig. 2), it is possible to implement the sum of the dc voltage sources (instead of a variable selection) and thus to synthesize $L = 2^N$ output voltage levels. The choice of a cascaded multilevel structure does not automatically imply the possibility of synthesizing at its output a higher number of levels L with respect to N input dc links: for example, for the converters in [13] and [16], multilevel structures are adopted with $L = N$, due to the choice of the input voltage source values and of the cell activation strategy.

By choosing a binary coding for V_{DC}^i values, the converter output voltage is a step waveform given by:

$$V_{out} = \sum_{i=1}^{N} b_i \frac{V_R}{2^i} + V_O \tag{1}$$

where b_i is the binary (b_i=1,0) controlling command of the *i-th* HB cell (see Fig. 2), $V_R = V_S \cdot 2^N$ is the reference voltage, V_S is the resolution and V_O is an arbitrary fixed voltage offset as shown in Fig. 2. The voltage swing ΔV of the circuit is between V_O and the maximum voltage V_M :

$$V_M = V_{out}^{MAX} = V_R\left(1 - \frac{1}{2^N}\right) + V_O \tag{2}$$

From (2), the minimum voltage resolution (*i.e.* when V_O = 0 V) is $V_S = V_M/(2^N - 1)$. This is an advantage with respect to commutated voltage sources architectures, which in the same conditions have a voltage resolution of $Vs = V_M/N$. The higher number of output levels provided by the proposed structure comes at the cost of higher switching rates with respect to a simple multilevel commutated-sources topology. Considering a full-scale sinusoidal input at frequency f_{in}, for our solution, only the switches of the most significant cell (*i.e.* the one with $V_{DC} = V_R/2$) commutate at f_{in}, while for the other cells the switching frequency increases. Indicating with i the cell order (i = 1 for the most significant cell/bit), the average commutation frequency of the *i-th* cell is [35]:

$$f_c = \left(2^{i-1}\right) f_{in} \tag{3}$$

This is not in contrast with the assumption that this multilevel solution can provide more bandwidth than traditional PWM Switched Mode Power Supply (SMPS): indeed, while for PWM SMPS the devices commutate at the maximum required switching speed with a switched voltage corresponding to the entire swing of the converter $\left(V_{DC} = V_{out}^{MAX}\right)$, in this case, for each

cell the commutated voltage V_{DC}^{i} is inversely proportional to the cell order *i*, hence to the switching frequency, and given by:

$$V_{DC}^{i} = \frac{V_R}{2^i} . \quad (4)$$

The switching losses, which are usually the most band-limiting factor, are considerably lower than in PWM SMPS, since the faster switching devices commutate dc link voltages whose values are rapidly decreasing with 2^i.

We chose to implement a converter suitable for the modulation of an RF HPA with up to 48 V maximum bias voltage (LDMOS or GaN amplifier). Since it is not convenient in terms of RF HPA efficiency to modulate the bias for the entire V_D swing (*e.g.* 0 - 48 V) [1], [14], and thus a fixed offset voltage V_O is always added to the dynamic bias, ΔV in the order of 40 V is the targeted voltage swing that must be covered by the dynamic part of our supply modulator.

By choosing $N = 3$, eight levels ($L = 8$) are used to cover the required dynamic range with a good compromise between circuit complexity and voltage resolution. Thus with $V_M = 48$ V and choosing for example $V_O = 6$ V, $\Delta V = 42$ V, $V_R = 48$ V and from (1) the correspondent input dc link voltages are $V_{DC}^{1} = 24$ V, $V_{DC}^{2} = 12$ V and $V_{DC}^{3} = 6$ V. The entire 48-V bias supply characteristic is covered with V_S= 6 V resolution and a fixed offset $V_O = 6$ V.

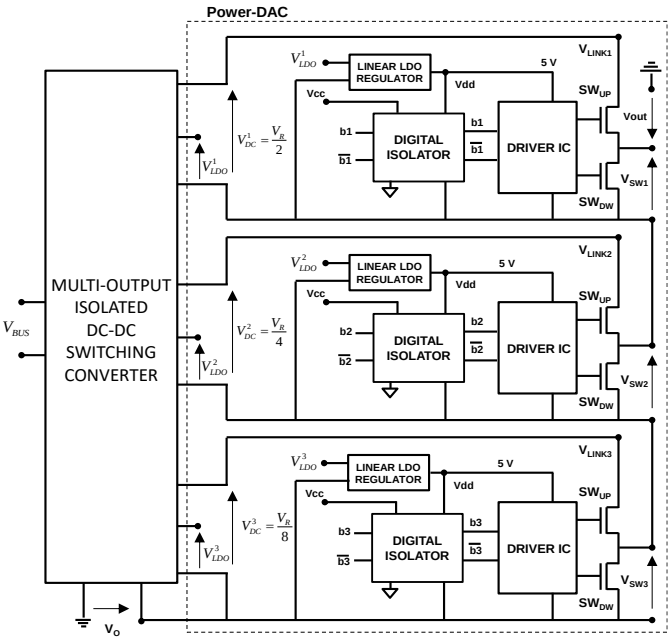

Fig. 3. Detailed structure of the proposed Power-DAC.

The detailed schematic of the Power-DAC is shown in Fig. 3. The three HB cells are implemented with two power switches (SW_{DW} and SW_{UP} in Fig. 3), driven by an integrated high-side/low-side driver. The power switches are GaN HEMT (High Electron Mobility Transistor) from EPC Corporation [34], [37]. This process implements a typical 2-DEG AlGaN/GaN HEMT heterostructure with field plate, grown on a silicon substrate. The device on-state resistance for this technology is equal to or less than state-of-the-art silicon power MOSFET technologies [34]. Low switching losses are obtained due to very low input and output device capacitances ensured by the lateral structure of the device, and due to the low threshold (about 1.6 V), which enables the device to be driven with only 5 V positive voltage. Finally, these devices feature flip-chip wafer-level bumped-die (no bonding wires) packages, whose dimensions are significantly lower than standard plastics packages for corresponding silicon MOSFET devices [34]. Taking also into account high electron mobility, switching times can be greatly reduced.

The device selected for the power switches is the EPC2014 [37] transistor, with the following main characteristics: R_{DSON} = 14 mΩ, VD_{BD} = 40 V, ID_{MAX} = 10 A, V_{GSTH} = 1.4 V, $C_{IN} = C_{GD} + C_{GS}$ = 300 pF, $C_{OUT} = C_{GD} + C_{DS}$ = 150 pF.

The maximum V_{GS} is 6 V, while 5 V is the optimum value for very fast switching. If suitably driven, the device can switch in about 2 ns. As can be seen in the Fig. 3, the power switches are controlled by an IC half-bridge driver circuit from Texas Instruments (LM5113), capable of driving both the high-side and low-side GaN devices of the HB cell. The IC includes the high-side and low-side CMOS totem-pole driver structures that guarantee very high switching speeds of the driven GaN FETs. The driver bias is V_{dd} = 5V and its output signals are very fast pulses with V_{OL} = 0 V and V_{OH} = 5 V, that are suitable to drive the GaN devices.

The isolated dc input voltage sources V_{DC}^{i} can be derived from the primary common supply voltage of the system (e.g. non isolated V_{BUS} = 48 V for a typical base station for telecommunications) by means of an isolated dc-dc switching converter with multiple output. The isolation requirement needs to be effective also in dynamic conditions, hence a multi-secondary transformer with low primary-to-secondary and secondary-to-secondary stray capacitances (*i.e.* < 250 pF) need to be selected [38]. A prototype isolated dc-dc converter, based on a multi output forward configuration with 94% efficiency was implemented to be used for the characterization of the Power-DAC. The need for a transformer for the isolation of the input dc links should not be considered as a disadvantage of this approach, since in the power supply system of a base station, isolated dc-dc converters from the non-isolated input voltage V_{BUS} (e.g. 48 V) are yet necessary [39] even for fixed bias supplies. Looking at Fig. 3, it can be noted that each driver IC is biased with V_{dd} = 5 V by a linear low-drop-out (LDO) voltage regulator (Microchip MCP1703), whose input voltage $V_{LDO}^{i} = 5.25$ V is supplied by an auxiliary low-power output of the multi-output isolated DC-DC converter. Due to its very low drop-out voltage this regulator works with 95% efficiency.

The dynamic isolation needs to be provided also for the controlling signals b_i: their isolation is obtained by exploiting compact capacitively-coupled digital isolators IC ISO7220M from Texas Instruments. These components guarantee dynamic isolation to dV/dt = 50 kV/μs, which is much higher than for conventional opto-couplers. The maximum bit rate is compatible with command switching frequency (150 MSPS). In each voltage level, the isolator is powered by the same linear regulator IC used for the driver.

III. Converter Design and Simulation

The design of the power section (drivers + HB cells) of the converter was carried out using two different CAD environments, exploiting time-domain simulation engines. First, the circuit operation was simulated with PSIM, using very simple and fast switch and driver models to verify its working principles; then, detailed SPICE models of both the driver IC and the GaN switches were imported into Keysight ADS CAD environment for more detailed time domain simulations.

In Fig. 4, the simulations in PSIM environment of the converter output voltage *Vout* corresponding to a 1 MHz full-scale (42 Vpp amplitude) input sinusoid is shown (V_O = 6 V not shown in Fig. 4). The drivers of the three HB cells are controlled by the three bits (b_1, b_2, b_3) of the quantized input sinusoid. In the lower part of the graph, the three digital inputs controlling the HB cells are shown: the commutation rate increases for the less significant bits as described in (3). Being f_{in} the frequency of the full-scale sinusoid, the bit (b_1, b_2, b_3) equivalent average switching frequencies are f_{in}, $3f_{in}$, $7f_{in}$ respectively (see (3)). The same simulations are shown in Fig. 5 for an arbitrary 10-MHz bandwidth, 42 V peak voltage, 12 dB PAPR signal. The sequences of the controlling bits in both Fig. 4 and 5, put in evidence that the commutation pattern of the switches is different from the one in a PWM converter. While for PWM the switching frequency (f_{SW}) is constant and the width of the pulses (*i.e.*, duty cycle) is proportional to the output amplitude, in this case, the switch state is determined by the instantaneous amplitude of the signal and by the quantization thresholds. Since there is not a fixed switching frequency, the typical bandwidth (BW) limitation BW< f_{SW}/10 of PWM converters [9], [17], [20], [26], [27] does not apply to the proposed circuit. The maximum bandwidth of the converter is determined by the shorter pulse achievable at the output: in the actual implementation, this limitation is not given by the very fast GaN switches, but by the drivers.

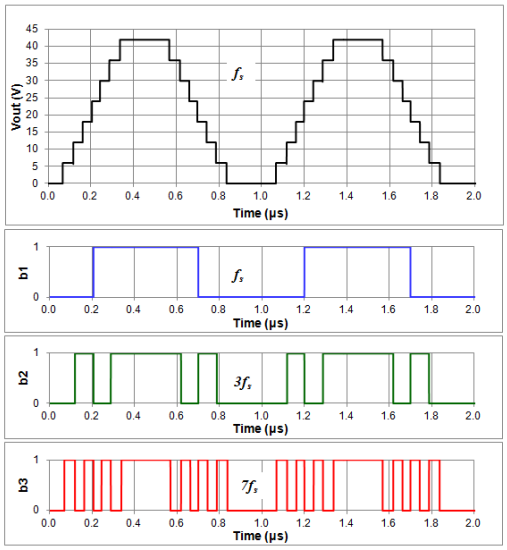

Fig. 4. Converter digital input signals and output response simulated in PSIM for a 1 MHz full-scale (42 Vpp amplitude) input sinusoid.

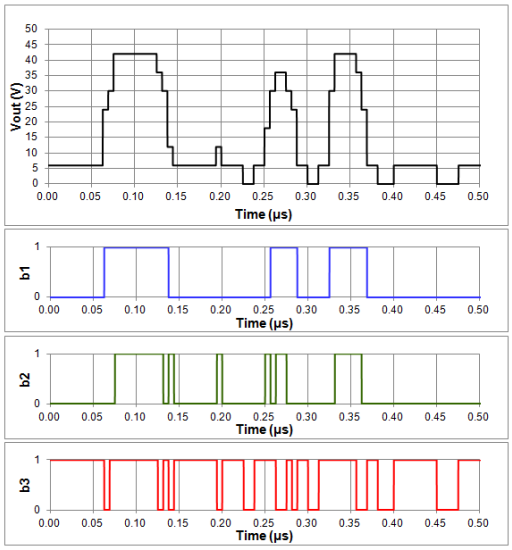

Fig. 5. Converter digital input signals and output response simulated in PSIM for an arbitrary 10-MHz bandwidth, 42 V peak voltage, 12 dB PAPR signal.

Indeed, the internal logic circuitry of the LM5113 driver limits the minimum pulse width at the driver output to 10 ns [42]: any shorter pulse at the input of the driver is simply discarded. As the number of commutations increases for less significant cells, this limitation is first faced by the highest order cell, when the input signal frequency gets high.

This loss of some commutations of the least significant bit is reflected in a loss of some voltage level transitions in the output waveform, when the input frequency f_{in} is above a certain value f_{in}^* (for a full-scale sinusoidal input).

Even though this effect does not really limit the operation of the Power-DAC, since it only decreases its ENOB (Effective Number of Bits) [35] (which is a common operation for DACs), for the actual implementation of the ET system with DPD, we chose to avoid this situation by implementing an optional preconditioning of the signal envelope (slew-rate limiting algorithm) before its amplification by the Power-DAC, as will be described in Section V.

We did not find in the market any faster driver IC optimized for 5 V operation, thus at the moment the only solution for faster operation is a dedicated design of integrated drivers. In Fig. 6, a schematic representation of the converter functionalities and the picture of the prototype are shown. Most of the prototype board space is unoccupied or used to place test pads: the real space needed for the Power-DAC can be estimated in the order of 11 cm^2. The digital isolator ICs, the driver ICs and the GaN FETs are soldered in the upper side of the board, while the linear regulators are placed in the backside. As shown in Fig. 6, the power section of the circuit (drivers + GaN switches) occupies a very limited area, due to the very high power density of GaN technology (GaN device dimensions are 0.8 mm x 1.6 mm).

The impact of the board layout with respect to path mismatches, parasitics and power/signal ground issues was taken into consideration during the board design. As a result, a very compact layout has been generated: a four layer PCB with a total thickness of only 0.8 mm was used for an optimum

distribution of ground planes and power signal paths. The minimization of series inductances in the gate drive loops was obtained by minimizing the distance between GaN devices and the driver ICs (LGA, Land grid Array, and BGA, Ball Grid Array, package technologies) and by exploiting low inductance micro-vias holes (150 µm diameter) to create short interconnections between the four PCB layers as suggested in [41]. This accurate layout design is fundamental to limit parasitics and signal misalignments that would cause relevant voltage spikes and ringings in correspondence with the fast commutations of GaN devices.

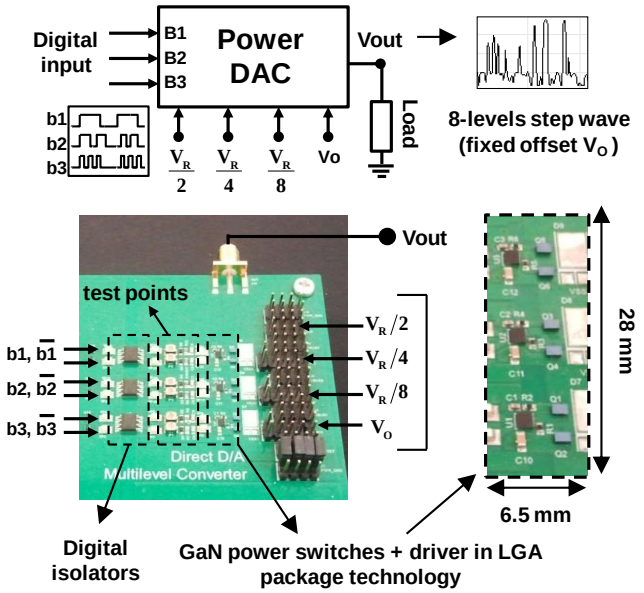

Fig. 6. Converter functional schematic and picture of the actual prototype.

As will be shown with in Section IV, the residual voltage glitches and ringings in the output waveforms can be highly suppressed by means of an output LC low pass filter. This filter placed between the supply modulator and the RF HPA has an important role in any type of ET architecture [27]. It is interesting to notice that, differently from the case of a PWM switching converter, in the proposed circuit the filter does not need to suppress the switching frequency, but rather to eliminate the mentioned glitches in the output waveform. Thus, the cut-off frequency of the filter can be quite high since these misalignments are on the order of 1-3 ns. The possibility to select small values for the filtering components, enables the implementation of a low impedance path between the HPA and the converter, whose behavior is similar in this way to an ideal voltage source. When selecting the filters for the different experiments proposed in section IV and V, the goal is the minimization of the commutation glitches, without compromising the converter bandwidth with a low cut-off frequency. Since with the selected LC filter topology, the 3-dB amplitude cut off frequency and the overshoot depend also on the load, different LC filters have been actually used for different experiments, as will be described in section IV and V.

IV. Measured Results with Resistive Load

The converter prototype was fully characterized with two different setups. In the first characterization set-up the Power-DAC was tested with different driving signals, when connected to a resistive power load R_{LOAD}. The digital input signals used in the tests were synthesized with an Altera Cyclone II FPGA [43]. Also the dedicated logic network used for the generation of a precise dead-time t_D between the two digital signals (b_i and $\overline{b_i}$) driving the complementary switches of each HB cell was implemented within the FPGA. The three dc link voltages V_{DC}^{i} selected for the tests were 6 V, 12 V and 24 V respectively, whereas the fixed offset voltage was not applied for this test (V_O = 0). The converter responses into R_{LOAD} = 30 ohm (about 24 W of output power) to full-scale sinusoid controlling signals at f_{IN} = 500 kHz, 1 MHz and 2 MHz are shown in Fig. 7: the output waveforms are measured before and after the output low pass filter. For this experiment, the LC filter is implemented with an SMD air-core inductor and ceramic capacitor with values L = 120 nH and C = 25 pF, that give a 3dB cut-off frequency response of the LCR_{LOAD} of about 50 MHz, without overshoots**.** The filter effectively suppresses the voltage spikes at supply voltage commutations (Fig. 7).

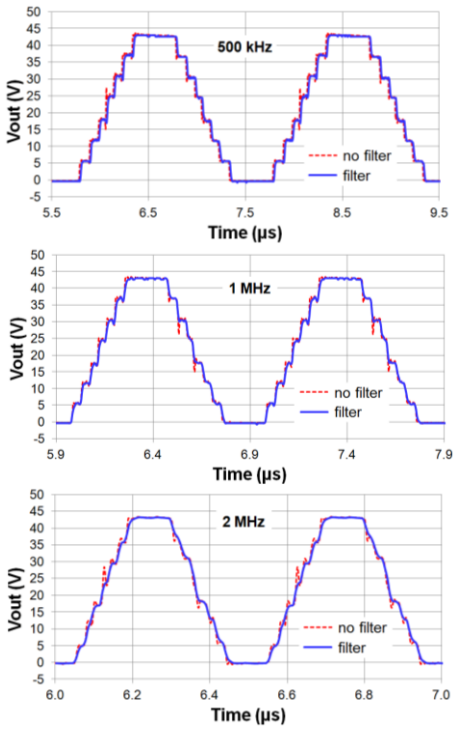

Fig. 7. Measured converter output with a full-scale sinusoidal set-point at different frequencies.

For the three experiments the average output power and peak power are P_{AVG} = 24.4 W and P_{PK} = 62.8 W respectively.

In Fig. 8, the measured performances in terms of efficiency (η) and power losses are listed. The losses of the driver circuits and their corresponding linear regulator were accurately evaluated by measuring the power consumption at the linear regulator inputs. The rest of the losses are ascribable to the GaN

FET, whereas their partitioning between conduction and switching losses was evaluated by time-domain simulations in ADS. The power losses breakdown proposed in Fig. 8(b) enables to distinguish between the efficiency of the GaN half bridge (HB) cells and the total efficiency of the converter, as proposed in Fig. 8(a). The measured efficiency of the converter is considerable and was found very close to simulations (1.2 points of efficiency was the maximum discrepancy).

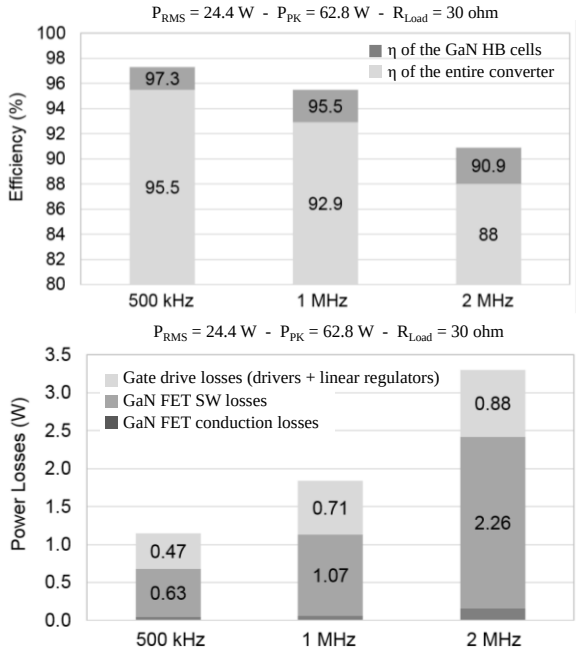

Fig. 8. Converter measured performance with full-scale sinusoidal inputs and power loss breakdown.

The full-scale sinusoidal input drive described in Fig. 7 and Fig. 8 represents the most demanding operation of the converter for the definition of its bandwidth and efficiency. This condition corresponds to the evaluation of the efficiency of the power converter with a driving signal exhibiting practically the total amount of its power concentrated at the upper limit of its bandwidth. This represent clearly a worst case, since all the practical signals for communication ET applications exhibit a distribution of the signal power that rapidly decreases for increasing frequencies [8], [12], [20] (typically 80% of the power is concentrated in the first hundred kHz of the bandwidth). Thus, the test proposed in Fig. 7 and Fig. 8 is very demanding and it could be taken as a reference for the evaluation of efficiency (or bandwidth) for any ET power supply.

The converter was further tested using input set-point waveforms calculated by applying and arbitrary supply shaping function to the envelope of three different wideband RF communication signals. To this aim, we have modeled the relationship between the HPA output power (P_{out}) and the required corresponding supply voltage (V_D) as $P_{out} = k \cdot V_D^{\,m}$. For RF HPAs, a good approximation can be obtained with m between 1 and 2: we chose k = 1 and m = 1.5 to describe the characteristic of a generic HPA. This choice gives the continuous characteristic (*i.e.* shaping function) $V_D = P_{out}^{\,2/3} = V_{ENV}^{\,4/3}$ (V_{ENV} is the envelope amplitude), which is then discretized with the eight levels of the Power-DAC, reasonably distributed within the HPA dynamic range, depending on the signal probability density function (*PDF*). Then the power-DAC set point is obtained by applying this discretized shaping function to the RF signal envelope, thus obtaining the corresponding sequence of 3-bit digital input commands to the Power-DAC. The three test bias set-points are calculated from the envelope of following RF signals: 1) 3GPP-WCDMA (Third Generation Partnership Project - Wideband Code Division Multiple Access) 4-MHz bandwidth signal with PAPR = 10 dB; 2) LTE 10-MHz signal with PAPR = 12 dB; 3) WiFi IEEE 802.11a 20-MHz 54Mbit/s signal with PAPR = 11 dB. Thus, the dynamic ranges and bandwidths of the test signals applied to the Power-DAC are particularly demanding, also considering the typical 2-4x multiplication factor between the bandwidth of the envelope with and the one of the original RF signal [1]-[10].

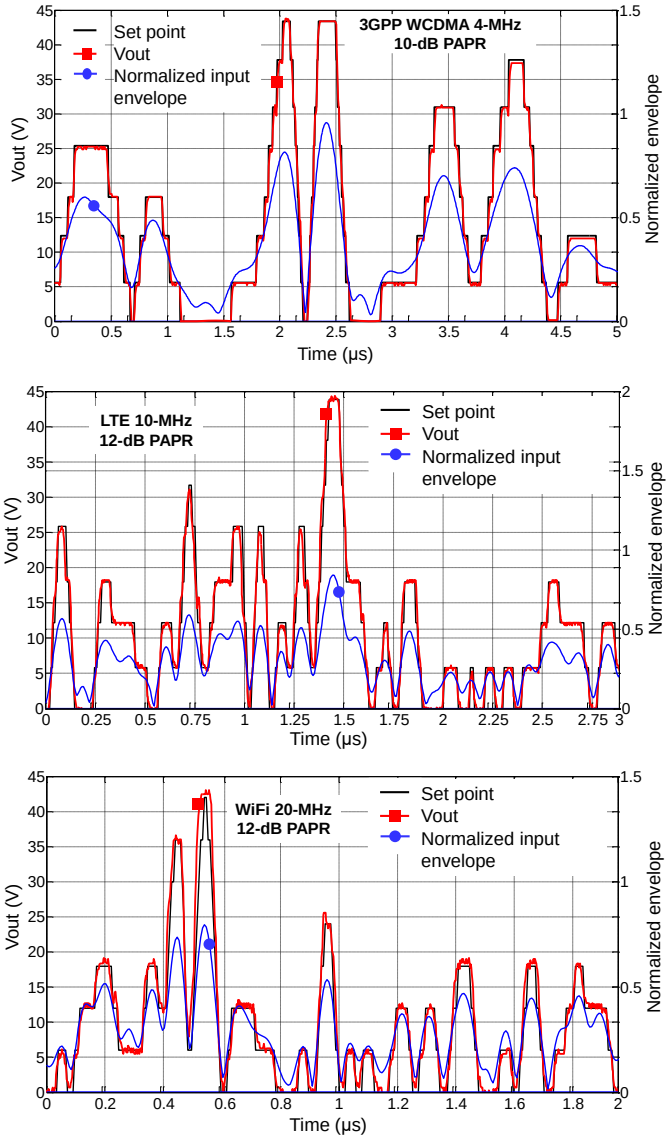

Fig. 9. Input RF signal normalized envelope, corresponding power supply ideal trajectory (set-point) and converter measured output (*Vout*) on resistive load.

TABLE I - COMPARISON WITH PUBLISHED CONVERTERS FOR ET AND EER APPLICATIONS

Ref	Application	Type	Switch technology	Test Signal / bandwidth	Pout average / peak	Slew-Rate	η
this work	ET	ML	40-V GaN	Full-scale 1 MHz Full-scale 2 MHz WCDMA / 4 MHZ LTE / 10 MHz WiFi /20 MHz	24.3 W / 62.8 W 24.3 W / 62.8 W 18 W / 159 W 16.57 W / 159 W 17.01 W / 159 W	4.23kV/μs	92.9% 88% 91.7% 84.5% 78.2%
[1]	ET	SMLA	Si FET	WCDMA / 4 MHZ	34 W / n.a.	n.a.	83.2%
[2]	ET	SMLA	n.a	WiMAX / 10 MHz	n.a. / n.a	n.a.	n.a.
[3]	ET	SMLA	n.a.	WiMAX / 10 MHz	20.1 W / n.a.	n.a.	69.0%
[4]	ET/EER	SMLA	30-V Si FET	WCDMA / n.a.	n.a. / n.a	100 V/μs	60.0%
[5]	ET	SMLA	n.a.	WCDMA / 4 MHz	66 W / n.a.	n.a.	64%
[6]	ET	SMLA	100-V Si FET	WiMAX / 10 MHz	46 W / n.a.	n.a.	70.1%
[7]	ET	SMLA	n.a.	LTE / 10 MHz	25 W / n.a.	n.a.	76.0%
[8]	ET	SMLA	20-V Si FET	LTE / 60 MHz	7 W / n.a.	n.a.	72.3%
[9]	ET	ML	100-V Si FET	Sine wave / 300 kHz	10 W / n.a.	n.a.	88.0%
[11]	ET	SMLA	Si FET	WLAN / 16.25 MHz	176 mW / 1W	n.a.	55%
[13]	EER	ML	Si FET	Sine wave / 1 MHz	22 W / 50 W	n.a.	75.5%
[16]	EER	ML	Si FET	Sine wave / 2 MHz	17 W / n.a.	800 V/μs	63.2%
[17]	ET	SMML	65-V Si FET	Half Sine wave / 10 KHz	20 W / 51 W	6 V /μs	92%
[18]	ET	SMMP	60-V Si FET	WCDMA / 4MHz	2.7 W / 13 W	560 V /μs	n.a.
[19]	ET	ML	40-V Si FET	Sine wave / 300 kHz	23 W / 46 W	n.a.	79.7%

SMLA: Switching Mode Linear Assisted - SMMP: PWM Switching Mode Multi Phase - ML: Multi level - SMML: PWM Switching Mode ML

In this case, the resistive output load is R_{LOAD} = 12 ohm in order to increase the output power. The optimization of the filter for this load was achieved with L = 42 nH, C = 20 pF, corresponding to a 3dB cut-off frequency response of the LCR_{LOAD} of about 50 MHz, without overshoots. In Fig. 9, the converter measured output voltage is shown, along with the input set-point and the corresponding RF signal envelope (normalized input envelope in Fig. 9).

It can be observed that the converter accurately follows the input set-points (the curves are practically indistinguishable, see the normalized root mean square (NRMSE) in Fig. 10) for all the three different test signals. Glitches and ringings in the voltage waveforms are very small due to the filter optimization for this load.

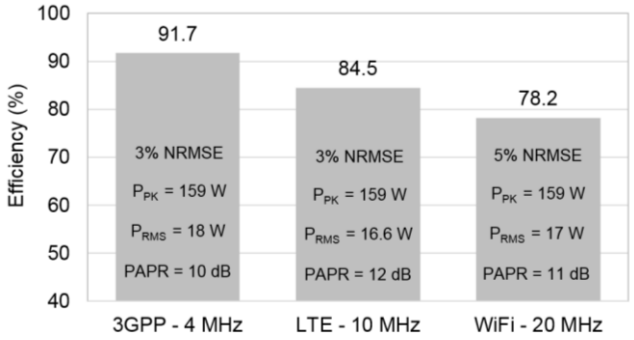

Fig. 10. Converter measured performance with input set-points derived from wideband communication signals (R_{LOAD} = 12 ohm).

The converter showed the capability of tracking these very large bandwidth signals, while maintaining high efficiency: indeed, in Fig. 10, the measured performances of the converter are listed for the three different input signals. The overall efficiency is very high considering the signal large bandwidths and PAPR of the signals; it decreases with increasing bandwidth as expected. Average and peak powers are P_{AVG} = 17-18 W and P_{PK} = 159 W, respectively. Simulations performed exploiting the thermal model of the GaN switches [37],[44] suggest that at least twice power levels can be delivered by the circuit with very similar efficiency by using heatsinks on the GaN switches, as in [45].

The efficiency of the Power-DAC scales with bandwidth, allowing greater flexibility compared with PWM SMPS, where the maximum bandwidth requirements set the fixed switching frequency and, therefore, the efficiency of the converter.

Another important parameter is the slew-rate of the supply modulator (combined with the dynamic range). The maximum large-signal slew rate of the Power-DAC was measured by commutating instantaneously the three HB power cells (42-V output voltage swing): due to the very fast commutating GaN devices, the measured slew rate is 4.23 kV/μs, which is extremely high if compared with many other published results as in [4], [16]-[18] and largely compliant with the requirements for communication signals [14].

The described performances of the Power-DAC have been compared with some state-of-the-art circuits. A fair and precise comparison between different products is practically impossible, since tests are made with different driving signals: nonetheless the performances of published converters for ET applications are listed in Table I. It is fair to notice that, in some papers, the efficiency calculation also includes the generation of the input dc link voltages (typically over 95%) and in some does not. The proposed circuit is certainly at the state of the art for these applications.

V. MEASURED RESULTS OF THE ENTIRE TRANSMITTER

A second set-up was developed for the characterization of the entire transmitter composed of the Power-DAC providing envelope tracking to an RF HPA. In this way the Power-DAC is tested under real operation and the possibility to avoid the use of a linear amplifier, by exploiting the DPD of the RF signal can be experimentally demonstrated. The set-up is described in Fig. 11 and it is based on the use of the Vector Signal Transceiver (VST) by National Instruments [46]: this

instrument is composed of a vector signal generator and a vector signal analyzer exploited for the characterization of the HPA with arbitrary modulated signals. In addition, the VST features an internal programmable FPGA with digital I/O channels, which can be used to generate real-time digital control signals or to apply dynamic parameter adjustments, synchronously with the RF signal generation and analysis. Thus, this FPGA was used for the digital control of the Power-DAC and the implementation of DPD of the RF signal, by developing proprietary codes (these codes are called VI, Virtual Instruments, in the LabVIEW programming environment).

The arbitrary in-phase/quadrature (I/Q) data are generated offline on a Host VI connected through a PXI-Express bus to the VST. As the data are downloaded on the FPGA, they begin to be processed by the blocks represented in Fig. 11. At each sampling instant, the calculated envelope, before entering the supply shaping table, is fed into a slew-rate limiter block, which implements the envelope algorithm presented in [47]. As mentioned in section III, the presence of this slew-rate limiter is necessary for the speed limitations of Power-DAC drivers (LM5113) [42], whose 10-ns minimum pulse width sets the upper bound to the maximum slew-rate of the Power-DAC for changing its output without losing any voltage transition. Thus, if necessary, the envelope is modified (slowed-down) by the slew-rate limiter in order to ensure a supply level application time in excess of the 10-ns limit.

As it is extensively described in [48], when this reduction of the supply waveforms bandwidth is applied, the overall efficiency of the transmitter can remain very high, since the degradation of the RF HPA efficiency can be compensated by the enhanced efficiency of the supply modulator. Moreover, also the additional distortion introduced by the bandwidth reduction can be compensated by DPD [48].

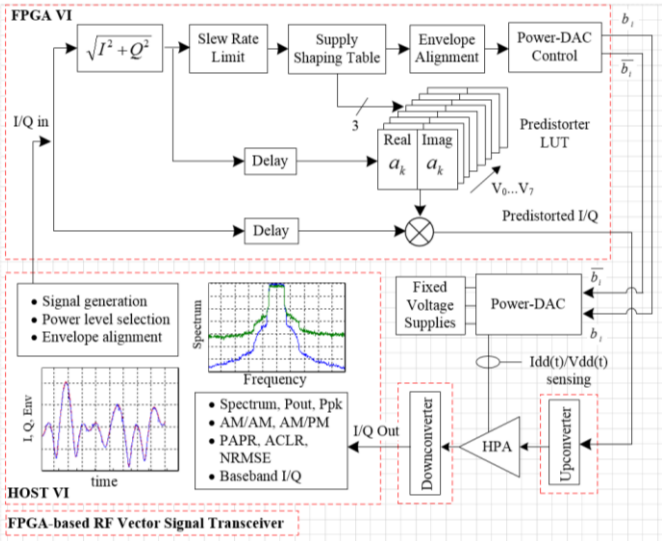

Fig. 11. Measurement set-up for the characterization of the RF HPA and the evaluation of the performance of the system with ET and DPD.

The conditioned envelope is then discretized by the shaping table for optimum RF HPA PAE, mapped inside a (look up table) LUT, whose output is the corresponding 3-bit digital input command provided in real-time to the Power-DAC through the instrument I/O digital channels. Also the DPD characteristics necessary for the HPA linearization are loaded as LUTs in the FPGA and are instantaneously applied to the input signal I/Q samples, synchronously with the ET digital commands of the Power-DAC.

A picture of the set-up is shown in Fig. 12. The HPA adopted for these tests exploits a 32-V LDMOS transistor for base station transmitter amplifiers. The HPA was designed at f_0 = 1.84 GHz central frequency and can deliver 45 dBm peak output power. For its implementation we adopted lumped SMD capacitors and microstrip structures on Roger RO4003C laminate; in particular, as can be appreciated in the picture of Fig. 12, the drain bias choke is implemented with a quarter-wave length stub.

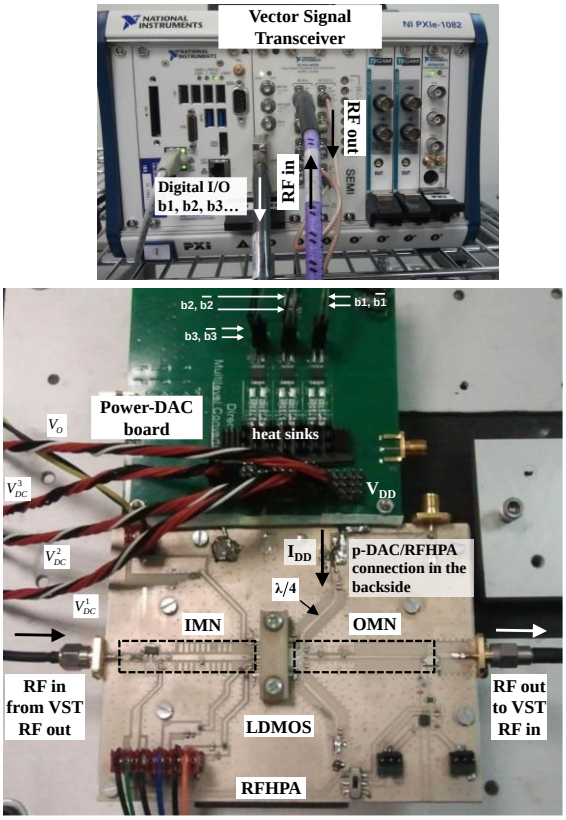

Fig. 12. Measurement set-up for the characterization of the RF HPA and the evaluation of the performance of the system with ET and DPD.

In this case the differential resistance of the HPA in operative conditions should be considered as the load of the filter between the Power-DAC and the HPA. At this stage, we did not perform this analysis on the HPA, but the filter has been selected with the following procedure: the capacitance at the drain of the HPA (*i.e.* the C element of the LC filter) has been minimized to C = 22 pF. This capacitance is dominated by the bypass capacitors placed at the drain supply port to attain HPA stability. The inductive part of the filter was minimized by implementing a very short connection between the power-DAC and the HPA board, as can be seen in Fig. 12. With this connection the estimated inductance is L = 12 nH. These values of L and C give a series impedance between the converter and the HPA of

less than 5 ohm in a 50 MHz bandwidth. As it will be shown in the following (measurements in Fig. 18), with this solution the commutation glitches in the drain voltage waveform at the HPA drain port are reasonably suppressed, even though there is still space for further optimizations.

For ET operation of the HPA with the Power-DAC, a fixed bias offset V_O = 8 V was chosen, while the binary-coded dc sources are $V_{DC}^1 = 13.7$ V, $V_{DC}^2 = 6.84$ V and $V_{DC}^3 = 3.43$ V: thus, the bias voltage swing 8-32 V is swept by the Power-DAC output signal with 3.43-V discretization steps (V_0 = 8 V, V_1 = 11.43 V, V_2 = 14.84 V, V_3 = 18.27 V, V_4 = 21.7 V, V_5 = 25.13 V, V_6 = 28.54 V, V_7 = 32 V).

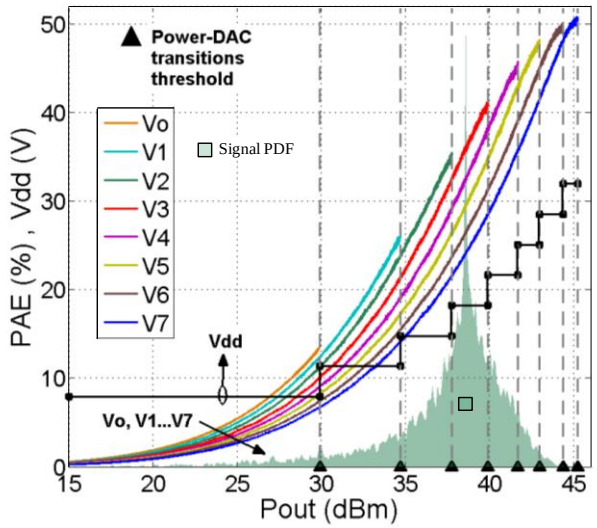

Fig. 13. Measured PAE of the HPA under test at different drain bias levels V_i and selected discretized supply shaping function $V_{DD} = \mathcal{F}_{\mathcal{D}}(P_{in})$.

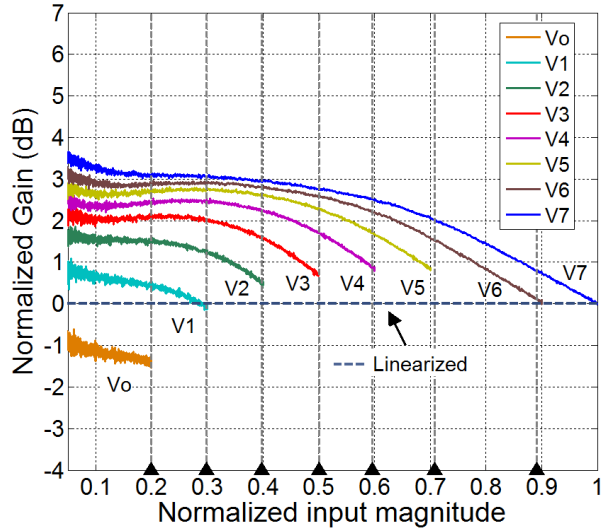

Fig. 14. Measured power gains of the HPA under test at different drain bias levels V_i, normalized to the HPA gain at maximum output power.

Exploiting the set-up in Fig. 11, the HPA was characterized in terms of RF output power, gain and PAE for the identification of the supply shaping function $\mathcal{F}_{\mathcal{D}}$ and the DPD characteristic. In Fig. 13, 14 and 15, the measured RF PAE, gain and output power characteristics of the HPA, sweeping the input power across its dynamic range for all the different bias levels V_i, are shown. These PAE, Pout and Gain maps are used for the selection of the RF input (or output) power threshold levels (*i.e.* input envelope amplitude), at which the supply voltage has to be switched to the next adjacent discrete value provided by the Power-DAC in order to track the optimum PAE regime.

These threshold levels need also to be compatible with the maximum correctable power of the HPA for each bias voltage level, which is limited by its saturation characteristic [49].

The vertical dashed lines in the graphs are the selected thresholds: practically, their positions within the HPA input dynamic range at variable bias voltages represent the supply shaping function $\mathcal{F}_{\mathcal{D}}$ for the HPA. In Fig. 13, also the resulting discretized supply shaping function $\mathcal{F}_{\mathcal{D}}$ implemented by the Power-DAC for the HPA under test is shown.

From the AM/AM and AM/PM measured characteristics (Fig. 15 and 16), a memoryless polynomial pre-distortion model for the linearization of the HPA working under ET operation was identified with an open-loop approach. The model is defined by (5), (6) and (7):

$$z(n) = \sum_{k=1}^{K_i} a_{k,i} x(n) |x(n)|^{k-1} \tag{5}$$

$$a_{k,i} = |a_{k,i}| e^{j\angle a_{k,i}} = a_{k,i}(V_i) \qquad i = 1...N \tag{6}$$

$$V_i = \mathcal{F}_{\mathcal{D}}(|x(n)|) \qquad i = 1...N \tag{7}$$

where $x(n)$ is the baseband signal at the HPA input before DPD and $z(n)$ is the baseband predistorter output. The complex polynomial coefficients $a_{k,i}$ depend on the instantaneous bias voltage V_i under ET operation, whereas V_i are selected by the input signal amplitude $|x(n)|$, according to the discretized shaping function $\mathcal{F}_{\mathcal{D}}$. The optimum polynomial order K_i has been found different for different V_i levels, with a maximum value of K_i = 9 (for i = 6,7). The number of complex coefficients of the model $a_{k,i}$ is $M = \sum_{i=1}^{N} K_i$. The model coefficients have been identified by complex polynomial fitting of the inverse of the AM/AM and AM/PM characteristics. This identification is performed in Matlab fitting eight complex polynomials (5) (one polynomial for each level V_i) to the measured characteristics by means of least square curve fitting.

In Fig. 15 and 16 the predistorter amplitude and phase characteristics respectively are shown: the predistorter characteristic provides the compensation of gain and phase variations (the gain steps can be appreciated in Fig. 14 or as slope variations in the AM/AM curves in Fig. 15), due to changing voltage levels, and of the HPA compression behavior within each voltage level.

As it is appreciable from Fig. 14 and 15, the adopted DPD linearizes the ET HPA for the gain at the targeted maximum power level $Pout_{pk}$, rather than for the maximum gain. As described in [49], with this choice the original and the pre-distorted inputs reach the same maximum power level and both the waveforms can be normalized to unity, simplifying the pre-distorter model identification and extraction. Nonetheless, with

this solution the average and peak output power of the linearized HPA are the same as in the case of linearizing for the maximum gain, thus the two DPD systems are equivalent in terms of linearization performance [49].

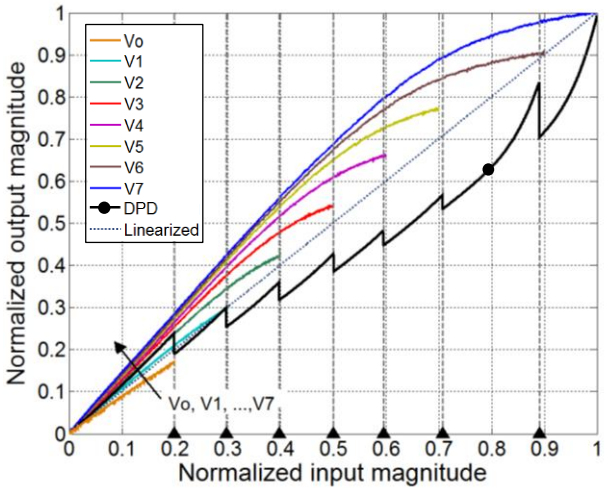

Fig. 15. Normalized measured AM/AM characteristic of the HPA under test at different drain bias levels V_i and predistorter amplitude characteristic.

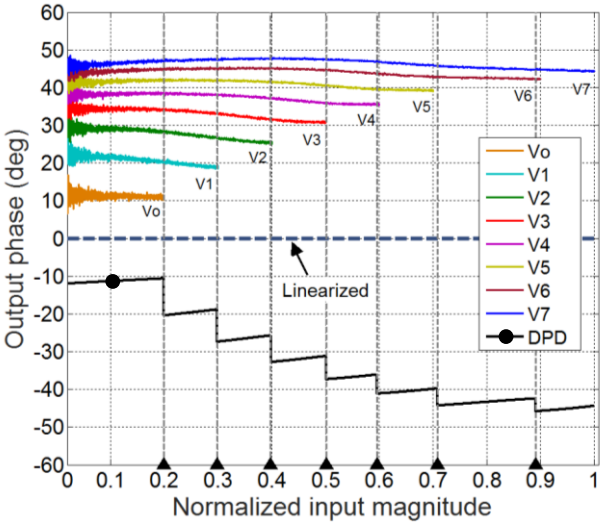

Fig. 16. Normalized measured AM/PM characteristic of the HPA under test at different drain bias levels V_i and predistorter phase characteristic.

The coefficients of the eight polynomials corresponding to the eight voltage levels V_i are stored in eight different LUT of the VST FPGA along with the shaping function $\mathcal{F}_{\mathcal{D}}$, as described in the block diagram of Fig. 11. For each sample of the input signal $x(n)$, its envelope selects through the shaping function the voltage level V_i to be applied. This voltage level defines also the polynomial to be used for the DPD. This implementation of the DPD function with multiple LUTs is not affected by discontinuity problems that could arise with a single predistorter function covering the entire dynamic range of the HPA.

The HPA performance are at first tested with a 1.4-MHz bandwidth, 7.5-dB PAPR LTE signal. The probability density function (*PDF*) of the test signal is shown in Fig. 13 with the HPA PAE curves and the selected shaping function $\mathcal{F}_{\mathcal{D}}$: a better optimization of $\mathcal{F}_{\mathcal{D}}$ with respect to the signal *PDF* can be surely pursued, following approaches similar to the ones described in [14], [50], [51] and will be the object of future activity. In addition to the considerations in [50], the discretization nature of the bias provided by the Power-DAC brings the further trade-off of the commutation-threshold positions within the HPA dynamic range: the simple variation of these thresholds, can decrease the number of commutation of the Power-DAC, whose consequent efficiency improvement needs to be evaluated in conjunction with the corresponding HPA PAE degradation.

The HPA has been characterized at four different regimes: in ET operation without linearization, in ET+DPD regime, at fixed V_{DD} with the same average input power Pin_{av} (V_{DD}^1) and at fixed V_{DD} with the same average output power $Pout_{av}$ (V_{DD}^2) as in the ET+DPD regime.

Measured data of these experiments are listed in table II. The most significant comparison is the one between fixed V_{DD} operation and ET+DPD regime with the same $Pout_{av}$ = 5.5 W (shaded columns in table II): since the HPA average gain is clearly reduced when operating in ET+DPD regime (due to both the variable V_{DD} of ET and the described linearization strategy), this condition at constant $Pout_{av}$ is achieved by decreasing the input signal average power Pin_{av} for the fixed V_{DD} regime (V_{DD}^2 in table II). This comparison shows an improvement of the HPA PAE from 24.4% to 41.6%, corresponding to a dc power consumption decreasing from 21.9 W to 12.48 W.

TABLE II– MEASURED SYSTEM PERFORMANCE WITH 1.4-MHZ LTE SIGNAL

		Fixed V_{DD}^1	Fixed V_{DD}^2	ET	ET+DPD
Gain		15 dB	15.4 dB	13.6 dB	12.6 dB
VDD	Max	32 V	32 V	32 V	32 V
	RMS	32 V	32 V	16.77 V	16.77 V
	Min	32 V	32 V	8 V	8 V
Pin_{av}		24.8 dBm	22 dBm	24.8 dBm	24.8 dBm
$Pout_{av}$		39.8 dBm	37.4 dBm	38.4 dBm	37.4 dBm
$Pout_{av}$		9.5 W	5.5 W	6.92 W	5.5 W
$Pout_{pk}$		44.7 dBm	43.8 dBm	44.9 dBm	45.1 dBm
Supply Power		28.5 W	**21.9 W**	14.46 W	**12.48 W**
HPA PAE		32.3%	**24.4%**	45.8%	**41.6%**
Supply Eff.		n.a.	n.a.	93.5%	92%
Congregate Eff.		32.3%	24.4%	42.8%	38.3%
ACLR	E-UTRA	-35.7 dB	-42.4 dB	-25.4 dB	-40.4 dB
	UTRA1	-61.1 dB	-60.7 dB	-40.1 dB	-49.9 dB
	UTRA2	-69.8 dB	-70.2 dB	-44.9 dB	-52.3 dB
NRMSE		10.74%	**7.3%**	27.8%	**4.2%**

E-UTRA: 970 kHz width, 1.2 MHz offset from f_0
UTRA1: 500 kHz width, 2.45 MHz offset from f_0
UTRA2: 250 kHz width, 3.825 MHz offset from f_0
V_{DD}^1: at the same Pin_{av} as ET - V_{DD}^2: at the same $Pout_{av}$ as ET

In this regime the Power-DAC works with a very high efficiency of 92%, providing a still considerable congregate efficiency $\eta = \eta_{HPA} \cdot \eta_{p\text{-}DAC}$ = 38.3% to the entire transmitter. In Table II, also the linearity performances are listed for both out-of-band (ACLR) and in-band (NRMSE) distortions. The implemented open-loop memoryless DPD is effective in compensating the additional distortion produced by the Power-DAC nonlinearity and the ET operation: the ACLR

improvement in the closest sideband (E-UTRA) is 15 dB and the NRMSE drops from 27.8% to 4.2%.

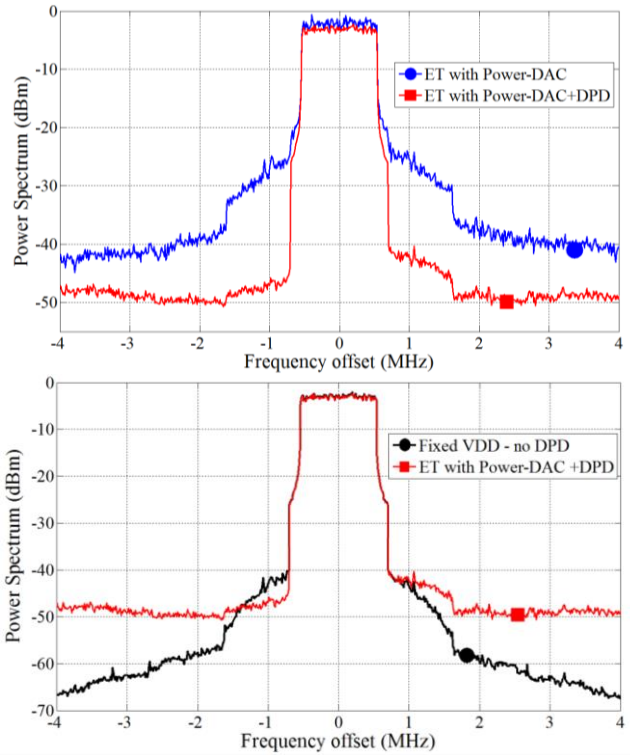

Fig. 17. Measured power spectra at HPA output for a 1.4-MHz, 7.5-dB PAPR LTE signal under different working regimes. Top: HPA output spectra under ET regime with and without DPD. Bottom: HPA output spectra under fixed bias (VDD = 32 V) and under ET+DPD regime at the same average output power $Pout_{av}$ = 37.4 dBm.

These effects of the DPD can be also appreciated in the graphs of Fig. 17 and 18. In the upper part of Fig. 17, the ACLR reduction provided by DPD to ET operation is shown; in the lower part of the figure, the comparison of spectra shows how the combination of ET and DPD is capable to provide ACLR performance very similar to the fixed VDD regime in the closest sideband (see also E-UTRA data in Table II), whereas it is also evident that at larger frequency offsets the noise in the spectrum is higher than with fixed VDD (see also UTRA1 and UTRA2 in Table II). In Fig. 18, a short time-window of the instantaneous normalized amplitude of the signal envelope measured by the VST at the input and at the output of the HPA in ET regime is shown, along with the corresponding dynamic bias voltage (sampled at the connection point between the Power-DAC and the HPA with an oscilloscope). These data are used for the calculation of the in-band distortion evaluated with the NRMSE [47]. The upper graph put in evidence the distortion introduced by the ET operation; in the lower graph, the linearizing effect of the DPD can be appreciated, ensuring the drop of the NRMSE from 27.8% to 4.2%. The dynamic bias voltage is unchanged in the two graphs, since the DPD is only applied to the I/Q of the RF signal, while the power-DAC operates in the same way in the two cases, since the supply voltage level is always switched on the bases of the non-pre-distorted signal envelope (see Fig. 11).

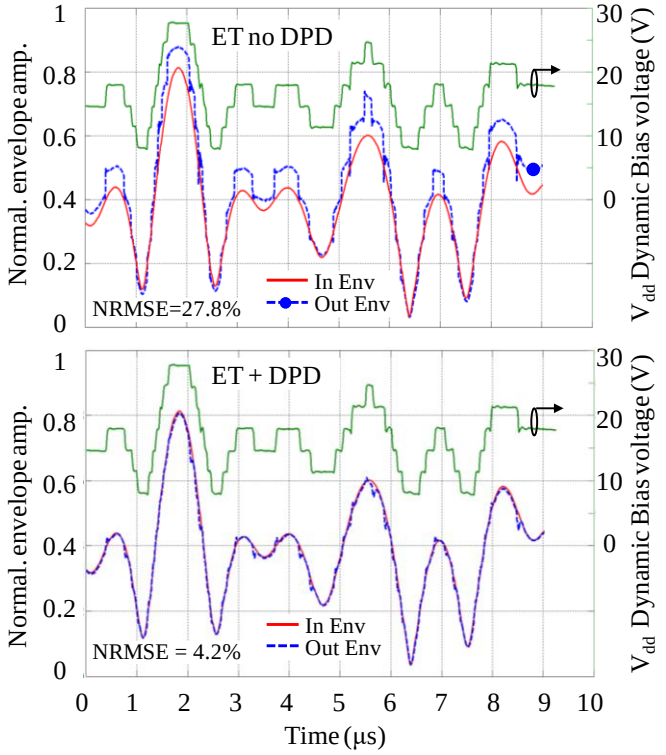

Fig. 18. Measured normalized amplitude of the time-domain signal envelope at the HPA input and output under ET operation with and without DPD and corresponding time-domain dynamic bias provided by the Power-DAC at the HPA drain bias port.

The same experiment was carried out with a 10-MHz bandwidth, 11.65-dB PAPR LTE signal. The results are shown in Fig. 19 and Table III. The HPA PAE improves from 10.9% to 28.8%, corresponding to a dc power consumption decreasing from 16.96 W to 6.28 W. With this wideband signal the Power-DAC works with a still high efficiency of 83%, providing 13 point of improvement of congregate efficiency for the entire transmitter. The ACLR improvement between ET and ET+DPD operations in the closest sideband (Table III) is 11 dB and the NRMSE reduces from 10.32% to 5.39%. As for the 1.4-MHz LTE signal, at larger frequency offsets the spectrum noise is quite higher than with fixed VDD.

The comparisons between the HPA output spectra with fixed VDD and with the ET+DPD operation presented in the lower graphs of Fig. 17 and 19, show that the main issue with the proposed approach is the noise performance in the far-out-of-band spectrum. This noise is mainly due to the commutation glitches shown in Fig. 18. The larger is the signal bandwidth, the bigger is the effect of these glitches, since their duration becomes more significant with respect to the symbol rate. This phenomenon is the main reason for the tradeoff between linearity and bandwidth of this approach.

While these glitches are practically eliminated (see Fig. 7 and 9) with the optimization of the LC filter response on a resistive load, it is much difficult to suppress them when the load is the variable differential resistance of an RF HPA. Nonetheless some optimizations of the connection between the Power-DAC and the RF HPA are still possible in order to reduce glitches and

thus the far-out-of-band noise. It has been experimentally observed that the glitches can be attenuated decreasing the bias-network bypass capacitance at the HPA drain. Moreover, the glitches could also be due to the non-perfect alignment of the supply and RF paths, which at the moment is implemented in the FPGA with a timing resolution of 8.3 ns: this is related, in the actual implementation, to the FPGA clock of 120 MHz, but can be reduced with some modification of the logic networks.

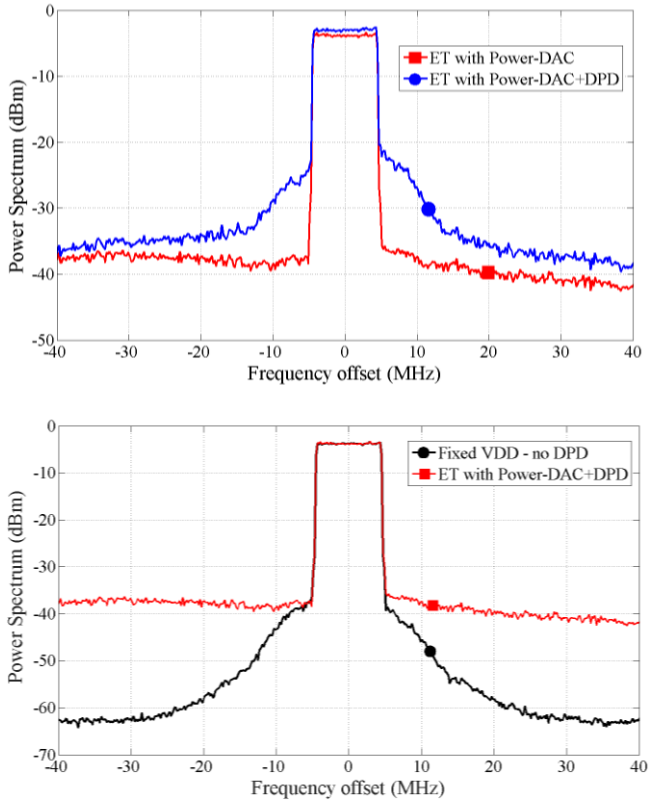

Fig. 19. Measured power spectra at HPA output for a 10-MHz, 11.65-dB PAPR LTE signal under different working regimes. Top: HPA output spectra under ET regime with and without DPD. Bottom: HPA output spectra under fixed bias (VDD = 32 V) and under ET+DPD regime at the same average output power $Pout_{av}$ = 32.8 dBm.

TABLE III– MEASURED SYSTEM PERFORMANCE WITH 10-MHZ LTE SIGNAL

		Fixed V_{DD}[1]	Fixed V_{DD}[2]	ET	ET+DPD
Gain		14.8 dB	15.1 dB	13.6 dB	12.8 dB
VDD	Max	32 V	32 V	32 V	32 V
	RMS	32 V	32 V	11.27 V	11.27 V
	Min	32 V	32 V	8 V	8 V
Pin_{av}		20 dBm	17.7 dBm	20 dBm	20 dBm
$Pout_{av}$		34.8 dBm	32.8 dBm	33.6 dBm	32.8 dBm
$Pout_{av}$		3.02 W	1.91 W	2.29 W	1.91 W
$Pout_{pk}$		43.9 dBm	43.0 dBm	44.6 dBm	44.5 dBm
Supply Power		20.48 W	**16.96 W**	6.75 W	**6.28 W**
HPA PAE		14.2%	**10.9%**	32.4%	**28.8%**
Supply Eff.		n.a.	n.a.	83%	83%
Congregate Eff.		14.2%	10.9%	26.9%	23.9%
ACLR	E-UTRA	- 38.0 dB	- 40.4 dB	- 25.4 dB	- 34.7 dB
	UTRA1	- 38.2 dB	- 40.5 dB	- 26.8 dB	- 37.8 dB
	UTRA2	- 44.6 dB	- 46.3 dB	- 30.5 dB	- 38.7 dB
NRMSE		3.67%	**2.65%**	10.32%	**5.39%**

E-UTRA: 9 MHz width, 10 MHz offset from f_0
UTRA1: 3.84 MHz width, 6.92 MHz offset from f_0
UTRA2: 3.84 kHz width, 10.76 MHz offset from f_0
V_{DD}[1]: at the same Pin_{av} as ET - V_{DD}[2]: at the same $Pout_{av}$ as ET

Finally some further in-band and in-near-sidebands linearity improvements can be achieved with the introduction of a DPD strategy with memory, which can take into account the memory effects introduced by the HPA within each bias level and in the transitions between different bias levels.

It is expected that these optimizations and the definition of a systematic procedure to identify the optimal discretized supply shaping function, based on the characteristics of the HPA and of the modulated signal (*i.e.*, PAPR and PDF), can bring even higher linearity and efficiency improvement to the transmitter.

VI. CONCLUSION

An envelope tracking (ET) transmitter architecture based on the combination of a novel digitally-controlled eight-level supply modulator and digital predistortion (DPD) has been proposed.

The power converter was tested on a resistive load using three input set-points suitable for wideband communication signals: 4-MHz 3GPP WCDMA, 10-MHz LTE, 20-MHz WiFi. In those conditions the circuit has shown to accurately follow the input set-points (NRMSE<5%), while operating with efficiencies of 91.7%, 84.5% and 78.2% respectively.

The complete ET architecture has been tested with an L-band LDMOS RF HPA with 1.4- and 10-MHz LTE signals with high PAPR. In these conditions the converter operates at 92% and 83% efficiency, respectively, whereas the congregate efficiency of the transmitter are 38.3% and 23.9%. These performances correspond to an improvement of 17.2 and 17.9 points for the power added efficiency (PAE) of the RF HPA and to 13.4 and 13 points of improvement for the efficiency of the entire transmitter.

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