Review of technology for normally-off HEMTs with p-GaN gate

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Abstract

Owing to the high carrier density and high electron mobility of the two dimensional electron gas (2DEG), high electron mobility transistors (HEMTs) based on gallium nitride (GaN) are suitable devices for high power and high frequency applications. Clearly, the presence of the 2DEG at the interface of AlGaN/GaN heterostructures makes HEMTs intrinsically normally-on devices. However, for power electronics applications, normally-off operation is desired for safety reasons and to simplify the driver circuitry. In this context, although several approaches to obtain normally-off transistors have been reported in the literature, normally-off GaN-based HEMTs with a p-GaN gate is among the most promising and the only commercially available today.

This paper reviews the most relevant technological issues for normally-off HEMTs with a p-GaN gate. First the operation principle and the impact of the heterostructure parameters are discussed. Then, the possible effects of the dry etching process of p-GaN are shortly mentioned. Thereafter, the role of the metal/p-GaN interface and the impact of the thermal processes on the electrical characteristics are widely discussed. Finally, recent alternative approaches proposed to avoid the use of the p-GaN dry etching are presented.

Keywords: normally-off HEMT, p-GaN, AlGaN/GaN heterostructures

1. Introduction

Gallium Nitride (GaN) and related semiconducting alloys (like AlGaN, InGaN, …) have been repeatedly mentioned as promising materials for the next generation of high-power and high-frequency electronics device [1,2,3]. In particular, High Electron Mobility Transistors (HEMTs) based on AlGaN/GaN heterostructures have superior performances with respect to their silicon (Si) counterparts, as they can operate at higher voltage, higher current, higher frequency and higher temperature [4], owing to the high electric field strength of the material combined with the high mobility and electron density of the two dimensional electron gas (2DEG) formed at the AlGaN/GaN interface [5].

Besides these intrinsic advantages, there is also a great interest in the possibility to grow AlGaN/GaN heterostructures on low-cost large-area (up to 200 mm) Si substrates, due to the enormous market potential and the possibility to integrate GaN power switches with the consolidated Si CMOS circuit technology [6]. Consequently, over the last decade, great efforts have been made to optimize the trade-off between the breakdown voltage (B_V) and specific ON-resistance (R_{ON}) of nitride-based transistors, e.g., working on the device geometry, reducing the defect density in the material and buffer layers, and developing new processing solutions for devices fabrication [7].

While normally-on AlGaN/GaN HEMTs are used for low-voltage and high frequency applications, for power switching applications normally-off characteristics are required to guarantee a safe operation and a simple gate drive configuration [8,9].

Several approaches have been proposed in order to obtain normally-off GaN-based HEMTs. In principle, the 2DEG depletion can be achieved using a thin AlGaN barrier layer with a low Al concentration. However, for an optimal device operation in terms of R_{ON}, the depletion of the 2DEG channel must be localized only below the gate, and it should be possible to completely restore the sheet carrier density through the application of a positive gate bias. Hence, the first

practical solution proposed for normally-off GaN HEMT has been the recession of the AlGaN barrier layer in the region below the gate electrode, by local plasma etch process [10]. Obviously, this approach requires an accurate control of the AlGaN etching technology. Moreover, the damage induced by the etching process could lead to an increase in the gate leakage current and to threshold voltage (V_{th}) non-uniformity effects. Hence, to improve the V_{th} uniformity and obtaining a low R_{ON}, a novel piezoneutralization technique has been proposed, which is based on the partial recession of a barrier layer composed by several AlGaN layers with different Al concentration [11].

On the other hand, the introduction of fluorine below the gate electrode has been also used to obtain normally-off operation. In this case, the negative charge of the F-ions, introduced either by plasma etch [12,13] or ion-implantation [14], promotes the depletion of the 2DEG channel, thus leading to a positive shift of threshold voltage V_{th} of the transistor. However, the V_{th} stability after high temperature annealing can be a concern in this kind of device [15].

Alternative but less diffused approaches to obtain a positive V_{th} shift include the local surface oxidation processes [16,17,18] or the introduction of a NiOx-based interlayer below the gate [19,20,21] .

To overcome many of the above limitations, the hybrid MIS-HEMT configuration has been proposed [22]. In this device, the AlGaN barrier layer is completely removed below the gate, forming the channel using a MIS system. Hence, this approach combines the advantages of a normally-off MIS channel with the low resistance of the 2DEG. However, the choice of the dielectric layer is extremely important in GaN devices [23,24], and in MISHEMTs it specifically impacts both the channel mobility [25,26] and threshold voltage stability [27].

Probably, the most promising approach is the use of a p-GaN (or p-AlGaN) layer on the AlGaN/GaN heterostructure under the gate contact region [28,29]. In this case, the p-GaN layer lifts up the band diagram, resulting in the depletion of the 2DEG channel even in the absence of an external applied bias (V_G=0). This process is receiving a great attention within the scientific community and, as a matter of fact, the only “real” normally-off GaN HEMT commercially

available to date are based on a p-GaN gate. Clearly, the technology of normally-off HEMT with p-GaN is rather complex, and the device behavior can be significantly influenced by several layout and processing conditions, which will be discussed in the present paper (e.g., choice of the heterostructure, selective p-GaN etch process, gate contacts, thermal budget, etc.). Obviously, there are other important reliability aspects associated to the normally-off AlGaN/GaN HEMT technology with a p-GaN gate, such as threshold voltage stability [30,34], charge trapping mechanisms [31], degradation processes induced by positive gate bias [30,32,33] or induced by high drain bias in off-state [34]. All these aspects are not treated in the present work as they have been widely discussed in another recently published review paper [34].

In this paper, the main technological issues related to the fabrication of normally-off HEMTs with p-GaN gate are reviewed. In particular, in section 2.1 after an introduction on the operation principle of the normally-off HEMT with p-GaN, the importance of the p-GaN/AlGaN/GaN heterostructure parameters (thickness, Al molar fraction, etc.) are discussed. Then, in section 2.2, the possible issues related to the selective plasma etch of the p-GaN are briefly illustrated. Thereafter, in section 2.3 the impact of the metal gate on the electrical behaviour of the normally-off p-GaN HEMTs is widely discussed. In particular, the choice metal gate work function and the p-GaN doping concentration, as well as the impact of the thermal annealing processes on the metal/p-GaN barrier are discussed, with a focus on the case study of a Ti/Al gate. Finally, in section 3 some recent alternative approaches to achieve normally-off p-GaN HEMTs without using of p-GaN dry etching are briefly mentioned.

2. Technological issues for normally-off HEMTs with p-GaN

2.1. Operation principle and impact of the heterostructure properties

The operation principle of the normally-off HEMT using a p-GaN gate is schematically depicted in Fig. 1. Basically, the use of a standard Schottky contact as gate electrode onto an AlGaN/GaN heterostructure leads to normally-on operation of the devices, as the AlGaN conduction band edge lies bellow the Fermi level at the interface with GaN. On the other hand, after the introduction of a p-GaN cap layer onto the AlGaN, the conduction band of the AlGaN is lifted up, thus leading to the depletion of the 2DEG. In this way, in principle, the normally-off operation of the device can be achieved.

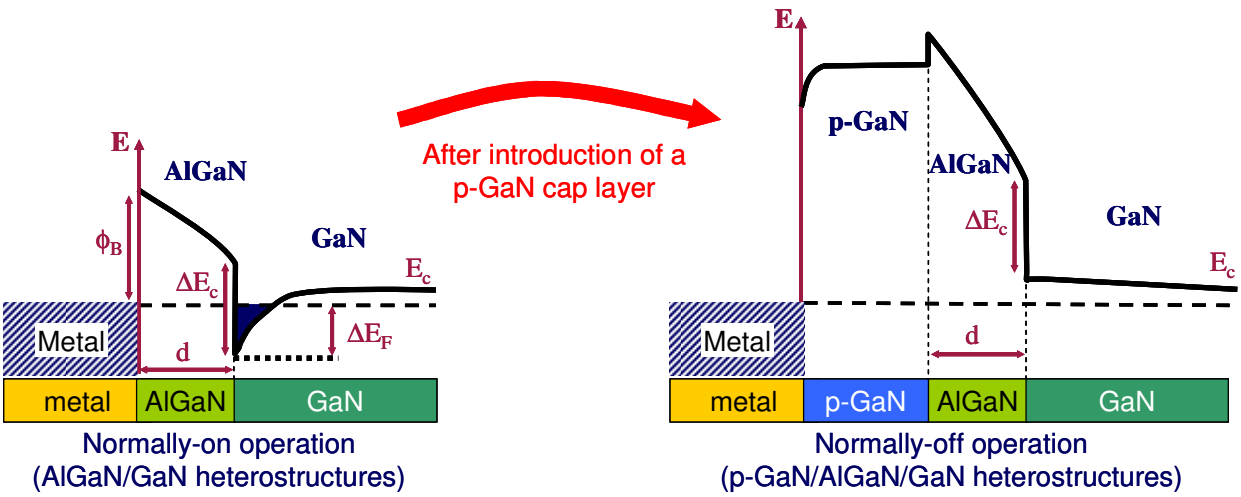

Fig. 1: Schematic of the operation principle of the normally-off HEMT with a p-GaN gate. As can be seen, the introduction of the p-GaN layer lifts up the conduction band of the AlGaN, leading to the depletion of the 2DEG.

However addition of any p-GaN capping layer on top of an AlGaN/GaN heterostructure not necessarily ensure normally-off operation. In fact, an appropriate choice of all the heterostructure parameters (i.e., acceptor concentration of p-GaN, residual donor concentrations in the AlGaN and GaN, thickness (d_{AlGaN}) and Al molar fraction (x_{AlGaN}) of the $Al_xGa_{1-x}N$ barrier layer, etc.) is fundamental in order to efficiently deplete the 2DEG channel and achieve a reasonable threshold voltage $V_{th.}$.

First of all, to facilitate the 2DEG depletion in the equilibrium condition (at V_G=0), a high acceptor concentration of the p-type GaN cap layer must be used. However, while an intrinsic n-

type conductivity is typically observed even in nominally undoped GaN or AlGaN [35], the achievement of a p-type conductivity in GaN has been a long standing problem [36]. Magnesium (Mg) is the reference p-type dopant for GaN or AlGaN, as it acts as an acceptor when incorporated in the nitride lattice in substitution of Ga. However, it is difficult to obtain a high holes concentration in p-GaN (or p-AlGaN), since the ionization energy of Mg p-type dopant is relatively high, i.e., in the range 150 - 200 meV [37,38]. Typically, p-type GaN cap layers with an acceptor concentration of about 3×10^{19} cm^{-3} are used, i.e., around three orders of magnitude higher than the residual donor doping concentration of the AlGaN layer. A higher Mg content in the p-GaN is not recommended, since its incorporation could lead to a deterioration of the crystalline quality of the layer and to a consequent decrease in the electrically active acceptors [39].

The thickness (d_{AlGaN}) and the Al molar fraction (x_{AlGaN}) of the $Al_xGa_{1-x}N$ barrier layer are two important parameters influencing the band diagram of the p-GaN/AlGaN/GaN heterostructure and, hence, the overall electrical behaviour of the system. Fig. 2a shows the simulated conduction band in the case of a p-GaN/AlGaN/GaN heterostructure, with an AlGaN thickness d_{AlGaN} = 25 nm and two different Al concentration values, i.e., x_{AlGaN} = 0.12 and x_{AlGaN} = 0.26 (a). A one-dimension Poisson-Schrödinger solver has been used to determine the energy band diagram. In particular, the thickness of the p-GaN layer was 50 nm and its acceptor concentration was $N_A = 3\times10^{19}$ cm^{-3}. As can be observed, in case of a higher Al molar fraction, the only presence of p-GaN is not sufficient to achieve a normally-off behaviour in the equilibrium condition (at $V_G = 0$ V), as the conduction band edge at the AlGaN/GaN interface lies still below the Fermi level. On the other hand, using a lower Al molar fraction of the barrier layer (x_{AlGaN} = 0.12) enables a more efficient depletion of the 2DEG (as the conduction band edge lies now well above the Fermi level), leading to a heterostructure suitable for normally-off operation. A similar behaviour can be observed in Fig. 2b, which reports the conduction band diagram of the p-GaN/AlGaN/GaN heterostructure with an Al molar fraction of x_{AlGaN} = 0.26, for two different AlGaN thickness values (d_{AlGaN} = 10 nm and d_{AlGaN} = 25 nm). In this case, a complete depletion of the 2DEG can be achieved only in the

heterostructures with the thinner AlGaN barrier layer (10nm). In this context, Fujii *et al.*[40] simulated the band diagram of p-GaN/AlGaN/GaN heterostructures by varying both the AlGaN thickness (d_{AlGaN}) and the Al molar fraction (x_{AlGaN}). In this way, it was possible to draw a "borderline" between heterostructures suitable for normally-off or normally-on operation, as can be seen in the plot reported in Fig. 2c. The separation line between the two operation conditions has been calculated considering the intersection point of the bottom of the conduction band with the Fermi level, in a d_{AlGaN} vs x_{AlGaN} graph. In the same graph, the symbols indicate the conditions simulated in Fig. 2a and Fig. 2b.

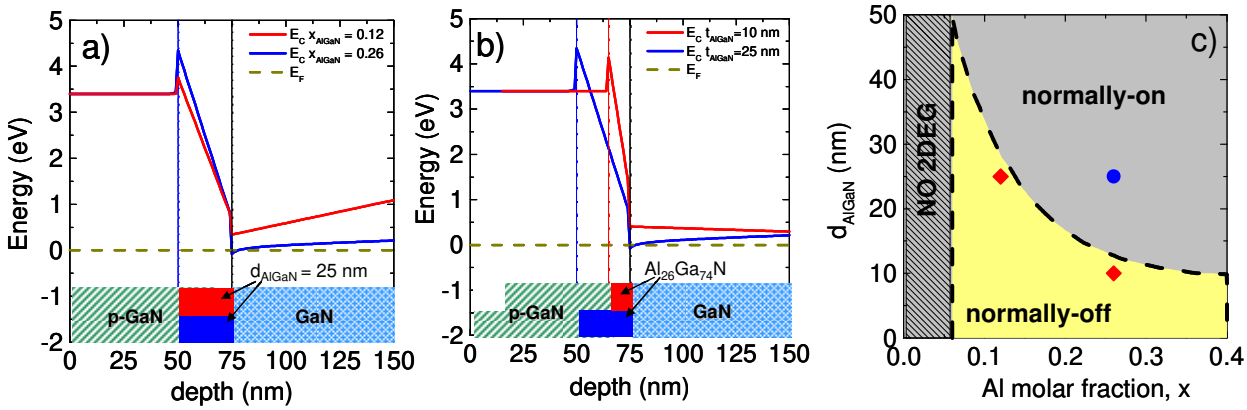

Fig. 2: Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure, for two different values of Al molar fraction (a), or two different values of the AlGaN thickness (b). The borderline between normally-on and normally-off operation mode as function of the Al molar fraction and AlGaN thickness in p-GaN/AlGaN/GaN heterostructures (c) based on the simulations performed in Ref. [40]. The data points reported in (c) refer to the conditions simulated in (a) and (b).

Following the first pioneering work by Hu *et al.* [41], a huge step forward in the technology of normally-off HEMTs with p-GaN gate was recorded in 2007 by Uemoto *et al.* [28], who demonstrated a normally-off device using a p-type AlGaN gate. In that work, they observed an interesting effect in the transfer characteristics of the devices, due to the injection of holes towards the interface, which give to the devices the name of Gate Injection Transistor (GIT).

Fig. 3 reports the transfer characteristics I_{DS}-V_G and the transconductance g_m of the GIT devices (

Fig. 3a) as well as a schematic of the device structure explaining the principle of operation (

Fig. 3b). From the transfer characteristics, a positive threshold voltage V_{th} of about 1.0 V can be estimated. Interestingly, two different peaks, at two different gate voltages, can be observed in the g_m curve. A schematic cross section of the of the p-AlGaN/i-AlGaN/i-GaN GIT is reported in

Fig. 3b, which graphically explains the current conduction observed in the three different regions (I, II and III) of the transfer characteristics. In particular, for $V_G < V_{th}$, the conduction band is below the Fermi level, the 2DEG is fully depleted and the device is off (region I). By increasing V_G up to the forward built-in voltage V_F of the p-AlGaN/i-AlGaN junction ($V_G < V_{th} < V_F$), the 2DEG is restored and the current flows from the source to the drain (region II). Finally, for higher bias values ($V_G > V_F$), holes start to be injected from the p-AlGaN to the 2DEG channel. Such mechanism is equilibrated by an equal injection of electrons from the source to the p-AlGaN gate to keep charge neutrality in the channel. These additional electrons move to the drain owing to the bias applied between source and drain (V_{DS}), while holes are kept around the gate electrode (region III). As a consequence, the drain current significantly increases maintaining a low gate current. Then, the presence of this second peak (region III) has been related to the holes injection occurred at higher gate voltage ($V_G > V_F$).

Here, it is worth noting that this effect in the g_m curves has been not so clearly observed by other authors. Moreover, most of the literature works are focused on the use of the p-GaN layer below the metal gate, instead of the AlGaN, since a more favorable band alignment permits a better depletion of the 2DEG. For that reason, in the remaining part of the manuscript only results obtained using a p-GaN gate will be presented.

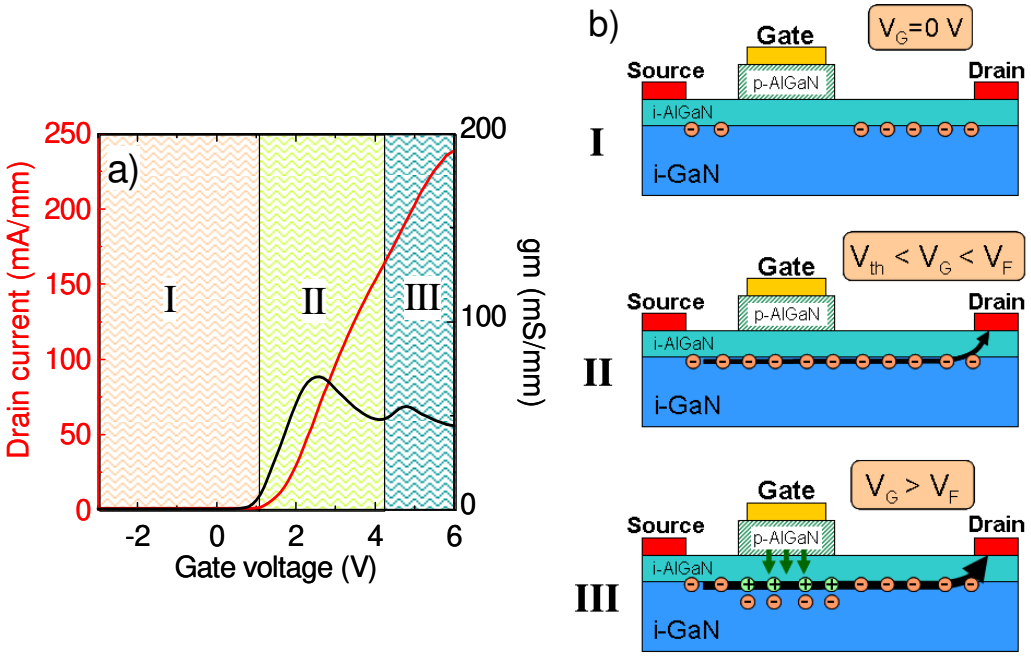

Fig. 3: (a) Transfer characteristics I_{DS}-V_G and transconductance g_m of the p-AlGaN/AlGaN/GaN Gate Injection Transistor (GIT) fabricated by Uemoto *et al.* [28]; the three different conduction regimes (I, II, III) are well distinguished; (b) Schematic cross section of the p-AlGaN/AlGaN/GaN GIT, explaining the electrical behavior of the device in the three different gate voltage conditions (regions I, II and III).

2.2. Selective plasma etch of the p-GaN

The selective etching of GaN over AlGaN, performed by Inductively Coupled Plasma (ICP) or Reactive Ion Etching (RIE), has received a great attention in GaN community in the last decades, due to the numerous applications in the fields of electronics and sensors [42]. In particular, these processes are required in the definition of the normally-off structure with the p-GaN gate, where the p-GaN cap layer must be selectively removed from the access regions and left only beneath the gate.

Obviously, several requirements must be fulfilled when dry etch is included in the flow chart for normally-off HEMT devices fabrication, like a smooth surface morphology, a low damage, a

controlled etch rate and a highly selective etching of one material with respect to another. This latter, in turn, depends on a variety of parameters, such as the gas chemistry, the ICP power, the chamber pressure, etc.

Several gas mixtures have been used to achieve selective GaN dry etch over AlGaN, all based on the presence of chlorine (Cl_2) as main etching agent e.g., Cl_2/Ar [43,44,45], $SiCl_4/Cl_2$ [46] and BCl_3/Cl_2 [47]. The characteristics of these processes, as for example the etch rate, can strongly change depending on plasma condition. Generally, the etch rate increases with increasing the ICP power of the process. Hence, ICP power must be reduced to have a better control of the etch rate, considering that the typical thickness of the p-GaN layer to be removed is in the range of 50-200nm. Han *et al.* [48] measured an etch rate about 400 nm/min for an ICP power of 1800 W using Cl_2/O_2 /N_2 based etch. In order to better control the process, this rate could be lowered down to 100 nm/min using lower ICP power (1000 W) [48]. A similar etch rate (around 100 nm/min) has been measured also for a Cl_2/O_2 /Ar mixture by Smith *et al.* [49], in spite of a significant reduction of the ICP power down to 300 W.

Another parameter that influences the etch rate is the chamber pressure. In particular, a lower chamber pressure could result in a faster etching process [48,49]. The values of the pressures typically used for GaN etching process are in the range of 5-20 mTorr.

Obviously, as specified in section 2.1, an optimal design for normally-off p-GaN technology requires the use of thin (10-25 nm) AlGaN layers, Hence, having a good selectivity of the p-GaN etch with respect to the AlGaN is extremely important, in order to avoid the degradation of the AlGaN surface in the access regions. In fact, the increase in the surface traps density in AlGaN due to plasma-induced damage can lead to a decrease in the concentration and/or mobility of the 2DEG, with the consequent increase in the transistor on-resistance.

In principle, starting from a plasma chemistry containing Cl_2 and O_2, the selectivity of GaN etch with respect to the AlGaN is expected, due to the higher binding energy of AlN (11.5 eV) compared with GaN (8.9 eV) [47], the higher affinity of oxygen to Al with respect to GaN [45] or the lower

volatility of $AlCl_x$ complexes with respect to $GaCl_x$ complexes [50,51]. Indeed, it has been demonstrated that the introduction of small amounts of O_2 in Cl_2-based dry etches increases the GaN etch rate [48] and improves the selectivity through the formation of an etch-resistant layer on the AlGaN surface [52]. Clearly, while on one side the selectivity is extremely important to avoid the removal of the AlGaN layer, on the other side a high etch rate can be difficult to control and high energy plasma could induce a damage on the AlGaN surface, thus compromising the device functionality. Therefore, in such cases a reduced etch rates are preferred in order to preserve surface morphology and the 2DEG properties..

As an example, Fig. 4a shows the results of our low power etch process, developed to remove a 50 nm thick p-GaN layer from the top of an AlGaN/GaN heterostructures with an AlGaN thickness of 10 nm and an Al concentration of 26%. The etching process has been performed using a Cl_2/O_2/Ar mixture and a chamber pressure of 5 mTorr, and an ICP power lower than 100 W (see Table I). In order to monitor the process, lithographic test patterns have been fabricated on the sample surface and then the step height has been measured by atomic force microscopy (AFM). A Ti/Al bilayer has been used as hard mask for the p-GaN etch. As can be seen in Fig. 4a, a good linearity of the etch rate is observed after stabilization of the plasma (after about 40 sec). The value of the etch rate determined from the measured step height and time was 13.2 nm/min, which is quite low with respect to other values reported in the literature. Although no selectivity with respect to the AlGaN has been observed, the slow etch rate and its linearity allowed us a very accurate control of p-GaN removal from the desired regions, as can be observed by the transmission electron microscopy (TEM) image shown in Fig. 4b .

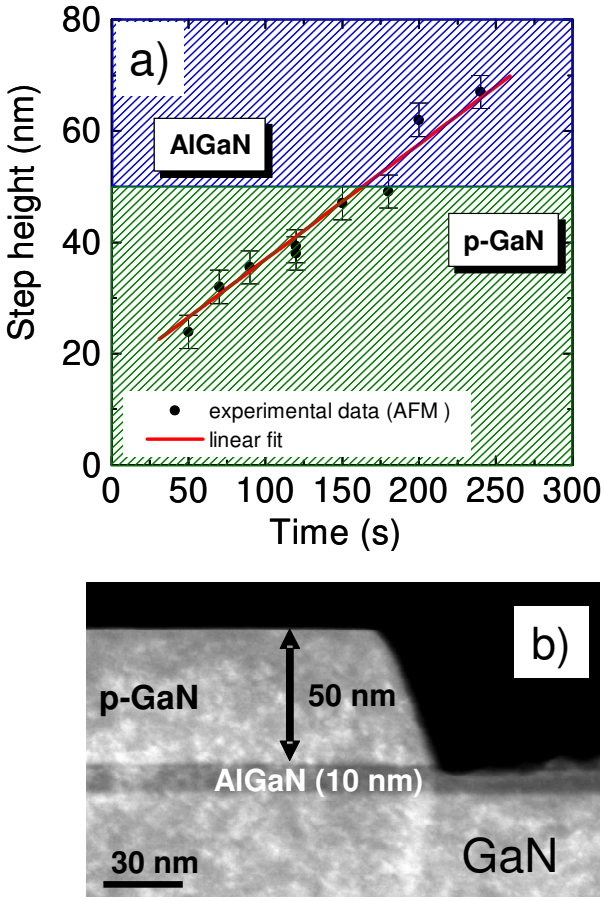

Fig. 4: (a) AFM measurement of the step height as a function of the etch time, used to calibrate the etch rate in the investigated p-GaN/AlGaN/GaN heterostructures; (b) Cross section TEM image of the p-GaN/AlGaN/GaN heterostructure after complete p-GaN removal from access regions.

p-GaN etching condition	
ICP equipment	Roth & Rau Microsys 400
ICP Power	100 Watt
Bias applied	250 V
Chamber pressure	5 mTorr
Gas based etch	$Cl_2/O_2/Ar$ (30/2/10 sccm)
Etching rate	13.2 nm /min

Table I: p-GaN etching conditions used to obtain the results shown in Fig. 4

Using this process, the low ICP power (<100W) and the consequent slow etch rate allow to preserve the surface morphology of the etched region. In particular, as can be seen on the AFM images shown in Fig. 5, the morphology of the AlGaN surface observed after the complete p-GaN removal exhibited a root means square roughness RMS = 5.5 nm, which was very similar to that of the original p-GaN surface (RMS= 5.0 nm). This controlled etch process has been used for the fabrication of normally-off devices with p-GaN gate, and the results will be described in section 2.3, where the Ti/Al hard mask has been also used as metal gate (to have a "self-aligned" process).

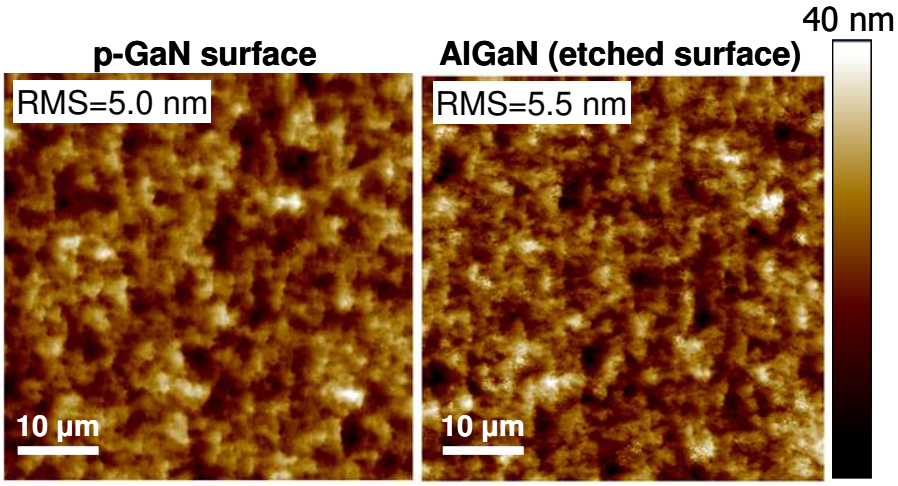

Fig. 5: Surface morphology, determined by AFM, of the p-GaN cap layer and of the AlGaN surface after the complete dry etching removal of the p-GaN, using the process described in Fig. 4 and Table I.

2.3 Metal contact for the p-GaN gate electrode

An important aspect in the technology of normally-off HEMT with a p-GaN gate is the metallization for p-GaN gate electrode. This issue has been discussed in several recent works, which reported on the influence of work-function of the metal for the p-GaN gate on the device electrical characteristics [29, 34,53,54,55].

In general, for a p-type semiconductor, according to the Schottky–Mott relation, the metal/semiconductor Schottky barrier height Φ_B obeys the relation:

$$\Phi_B = E_g - (\Phi_m - \chi_s) \quad (1)$$

where E_g is the bandgap of the semiconductor, Φ_m is the work function of the metal, and χ_s is the electron affinity of the semiconductor.

According to Eq. (1), the metals with a lower work-function should give a higher barrier height, while a lower barrier height should be obtained when using metals with a higher work-function. Fig. 6 shows a survey of experimental literature values of the Schottky barrier height at metal/p-GaN interfaces, reported as function of the metal work-function. From this plot, a clear correlation between the Schottky barrier height Φ_B with the metal work function Φ_m is observed, thus indicating that the Fermi level is not completely pinned at the surface. In particular, from linear fit of the experimental data reported in Fig. 6, an interface index S = - 0.7 can be calculated from the slope of the fit ($d\Phi_B/d\Phi_m$), which is lower with respect to the theoretical one (S = - 1) predicted by the Schottky–Mott relation (Eq. (1)). Hence, it can be concluded that the experimental value of the metal/p-GaN barrier height does not depend only on the metal-work function but also on the processing condition (surface preparation, material defects, annealing, etc.).

Typically, metals with a lower Φ_m (e.g., Ti, Al or W) are used for Schottky contact formation [56,57, 58]. On the other hand, Ohmic contact formation on p-GaN is generally obtained with metal with a higher Φ_m, e.g., Ni, Pd, Au or their combination [59,60]. However, the high metal work-function is not the only requirement for the formation of Ohmic contacts to p-type GaN with low specific contact resistance. In fact, often thermal treatment in oxidizing atmosphere could be necessary [59,61,62,63], which in turn can lead to a degradation of the 2DEG electrical properties [17,18].

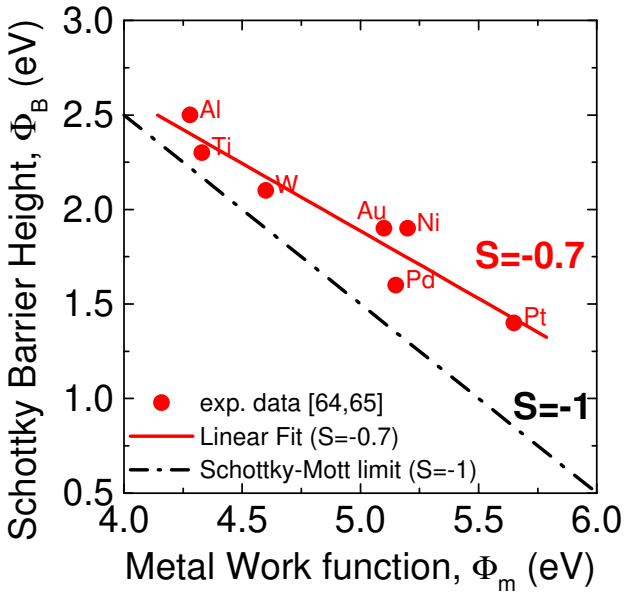

Fig. 6: Survey of experimental literature values of the Schottky barrier height (Φ_B) as a function of the metal work-function (Φ_m) for different metals on p-GaN. The data are taken from Refs. [64,65]. A linear fit of the data gives an interface index S = - 0.7. The dashed line indicates the theoretical behavior (S = - 1) predicted by the Schottky-Mott relation.

In this context, the choice of the metal gate in normally-off HEMTs with p-GaN gate represents still a debated topic. Uemoto *et al.* [28] used a Pd-based Ohmic contact as metal gate on the p-AlGaN cap layer, in order to improve hole injection effect at the basis of their GIT device (see section 2.1). On the other hand, Hwang *et al.* [29] used Schottky contacts in their normally-off HEMT, showing that a lower work-function metal (W) allows to increase the threshold voltage V_{th} with respect to a higher work-function one (Ni) and, at the same time, enables a reduction of the gate leakage current [29].

More recently, Meneghini *et al.* [34] compared the behavior of normally-off HEMTs with p-GaN gate, employing either an Ohmic or a Schottky metal gate. In particular, they showed that replacing a standard Ni/Au Ohmic gate contact with a Schottky gate contact based on a WSiN metallization enables to increase the transistor gate voltage swing up to 8 V (i.e., higher than the 6 V achieved

with p-GaN Ohmic contact) and to reduce the gate leakage current in ON-state about four orders of magnitude (see Fig. 7a and Fig. 7b).

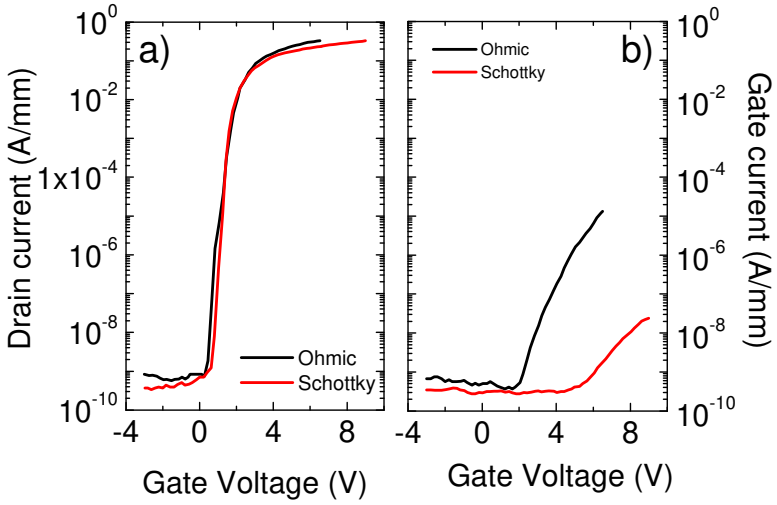

Fig. 7: Transfer characteristics (a) and gate current (b) as a function of the gate voltage for p-GaN-gate transistors with Ni/Au based Ohmic gate contacts (black) and WSiN based Schottky contacts (red) for a V_{DS} = +10 V. Using a WSiN Schottky gate on p-GaN allows to increase the gate voltage swing and to reduce the gate leakage current in the ON-state. The figure is adapted from Ref. [34]

As a matter of fact, TCAD simulations confirmed that a metal gate with a lower work-function Φ_m (i.e., resulting in a higher barrier Φ_B) gives a higher threshold voltage V_{th} and lower leakage current [29]. However, the large threshold voltage difference (ΔV_{th} = 1.8 V) observed between the device using Ni (Φ_m = 5.7 eV, V_{thNi}=1.3 V) and that using W (Φ_m = 4.7 eV V_{thW}=3.1 V), cannot be simply attributed to difference between the two metal work functions ($\Delta\Phi_m$ = 0.6eV), but it can be rather explained considering the voltage drop at the interface depletion region. In particular, the hole depletion region generated at the metal/p-GaN interface increases in thickness with decreasing metal work-function (due to the increase in the barrier height). Then, in the device with a metal gate of lower Φ_m, an applied positive gate bias will partially drop on a wider depletion region, thus leading to a higher V_{th}. On the other hand, in the device with a metal gate of higher Φ_m, the voltage drop on the thinner depletion region is quite negligible, similarly to the situation occurring in an

Ohmic contact. Hence, in this latter case a lower V_{th} is obtained. At the same time, since low work-function metals give a high barrier height, their use also results in a reduced gate current coming from the 2DEG channel.

In this respect, the doping of the p-GaN is another important parameter in the device design, as it influences the thickness of the depletion region at the metal/p-GaN interface. In Fig. 8, the conduction band of the p-GaN/GaN/AlGaN heterostructure has been simulated by a one-dimension Poisson-Schrödinger solver for two different p-type doping concentrations, i.e., $N_A = 1\times10^{17}$ cm^{-3} and $N_A = 1\times10^{19}$ cm^{-3}. As can be seen, the depletion of the 2DEG channel is not observed for the lower p-type concentration. On the other hand, the higher doping concentration allows the p-GaN to shift the conduction band above the Fermi level and makes the heterostructures suitable for normally-off operation.

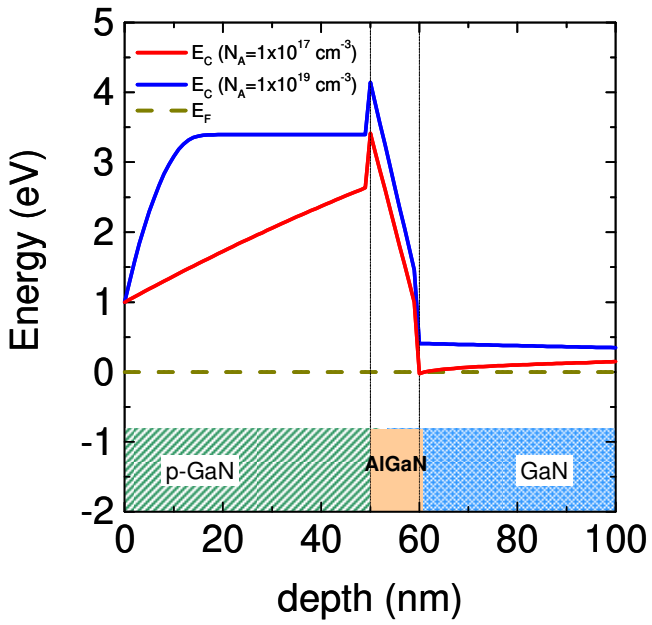

Fig. 8: Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure, for two different type doping concentrations of the p-GaN layer, i.e., $N_A = 1\times10^{17}$ cm^{-3} (red line) and $N_A = 1\times10^{19}$ cm^{-3} (blue line).

Efthymiou *et al.* [55] carried out a systematic simulation work on the optimization of the p-GaN layer properties for normally-off behavior. In particular, they confirmed that a high doping level N_A can guarantee a more efficient depletion of the 2DEG. Hence, an increase in the threshold voltage

V_{th} with increasing N_A is initially expected. However, this trend is inverted above a certain doping level of the p-GaN layer ($N_A > 1\times10^{18}$ cm^{-3}), where the metal/p-GaN interface becomes very narrow and the applied bias does not drop across the depletion region, similarly to what happens in case of Ohmic contacts [55].

All the above considerations point out that the metal/p-GaN interface (i.e., doping concentration, barrier height) play a relevant role on the electrical performance of the normally-off p-GaN HEMT.

However, the barrier height Φ_B does not depend only on the metal work-function (as confirmed by the value of the interface index found in Fig. 6) but it can be influenced by several other conditions, e.g., semiconductor surface defects, metal deposition technique, surface preparation, annealing conditions, etc.. Among them, the thermal budget needed to achieve Ohmic contact formation in AlGaN/GaN heterostructures can have a significant influence on the electrical behavior of the p-GaN HEMTs [53]. In order to investigate this aspect, we firstly fabricated a normally off p-GaN HEMT using p-GaN/AlGaN/GaN heterostructures, with a p-GaN cap layer 50 nm thick, an AlGaN layer with a thickness of 10 nm and an Al content of 26 %. The metal gate was fabricated using a Ti/Al bilayer above the p-GaN ($N_A=3\times10^{19}$ cm^{-3}) in order to obtain a higher Φ_B. Fig. 9 reports the electrical output characteristics (I_{DS}-V_{DS}) and the transfer characteristics (I_{DS}-V_G at V_{DS}=10V) of the fabricated device. As can be seen, the transistor exhibits a normally-off behavior with a pinch-off voltage of +1.1 V and a V_{th} = +1.5 V, as calculated from the linear fit of $I_{DS}^{1/2}$ vs V_G plot. In this case, the gate voltage swing was enhanced up to 10 V, i.e., higher than the values reported in Fig. 7.

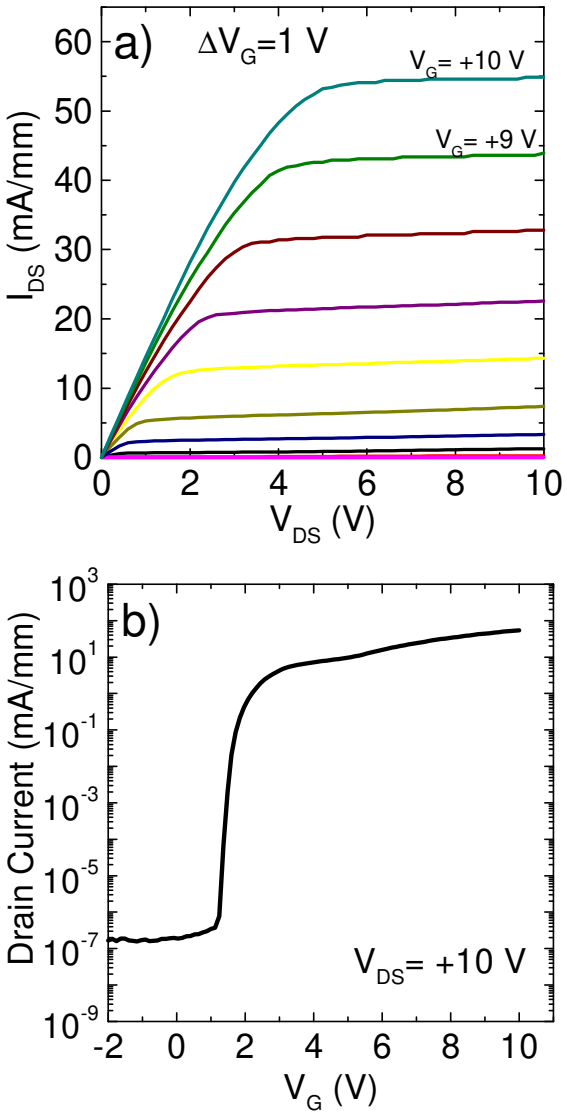

Fig. 9: (a) I–V output characteristics and (b) transfer characteristics of the p-GaN/AlGaN/GaN HEMT with a Ti/Al metal gate.

To optimize the device fabrication flow-chart, a “self aligned” process for the metal gate definition can be adopted, i.e., using the same metal firstly as hard mask for the p-GaN etch and, then, as device gate electrode. However, under these conditions, the metal gate have to be subjected to thermal annealing processes (e.g., at a temperature of about 800 °C) for Ohmic contact formation.

In order to evaluate the effect of the thermal budgets on metal/p-GaN gate and, hence, on the HEMT electrical behavior, the fabricated device was annealed at 800 °C in Ar atmosphere for 1

min. The impact of this annealing process is summarized in Fig. 10. In particular, after annealing worse device electrical characteristics are observed, as can be deduced from the negative shift of the threshold voltage V_{th}, which moved from +1.5 V to -0.6 V (see Fig. 10a). Moreover, a considerable increase in the gate current of about six orders of magnitude is also observed in the annealed sample (see Fig. 10b). As a consequence, also the gate voltage swing of the device is seriously limited in this annealed device.

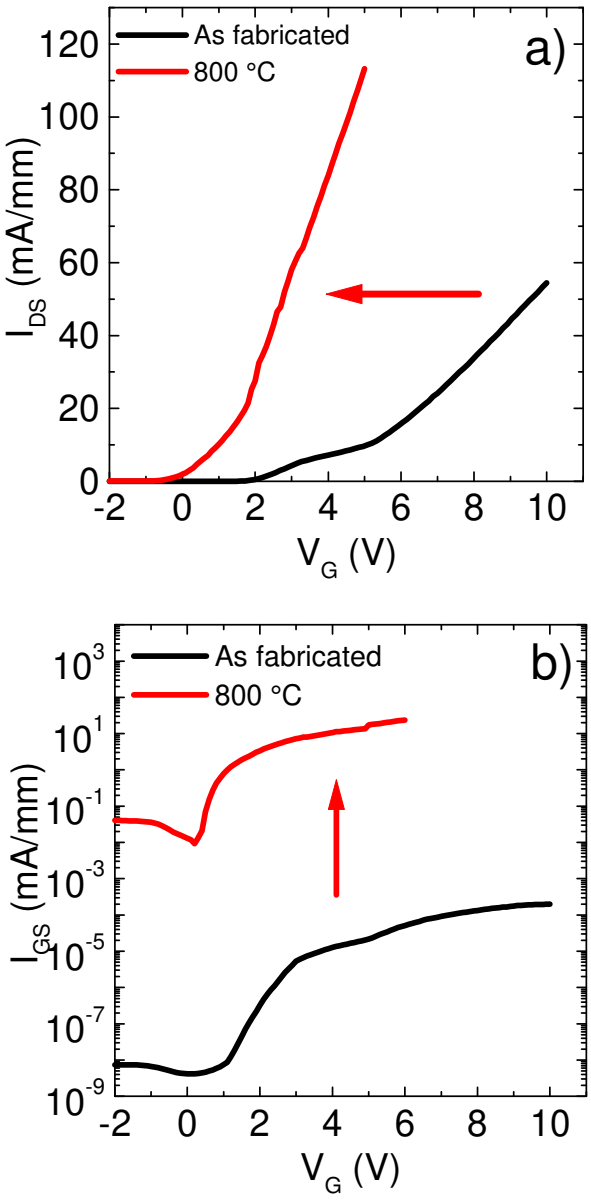

Fig. 10: (a) Transfer characteristics and (b) gate current as function of the gate voltage V_G measured in the as fabricated (black line) and 800 °C annealed (red line) p-GaN/AlGaN/GaN HEMT with a Ti/Al metal gate..

A possible explanation of this electrical degradation could be given by monitoring the modification of the metal/p-GaN interface during annealing treatments. For this purpose, "back-to-back" test-patterns [66,67,68] have been fabricated on blanket p-GaN layers in order to determine the value of the barrier height of the Ti/Al gate, as schematically shown in Fig. 11a. This kind of structure consists in the series of two Schottky contacts, one in forward and another in reverse configuration. Then, at low bias (e.g., $V < 0.8$ V) the current is limited by the high interface resistance of the Schottky contact biased in reverse configuration (R_1 or R_2). Conversely, at higher bias values, the contribution of the material resistivity (R_B) becomes predominant [69,70].

The I-V measurements acquired in the back-to-back contacts are shown in Fig. 11b, for three different annealing conditions, i.e., as deposited, 400 °C and 800 °C annealed samples. As can be observed, the as deposited contacts show the lowest leakage current, which in turn significantly increases with increasing the annealing temperature.

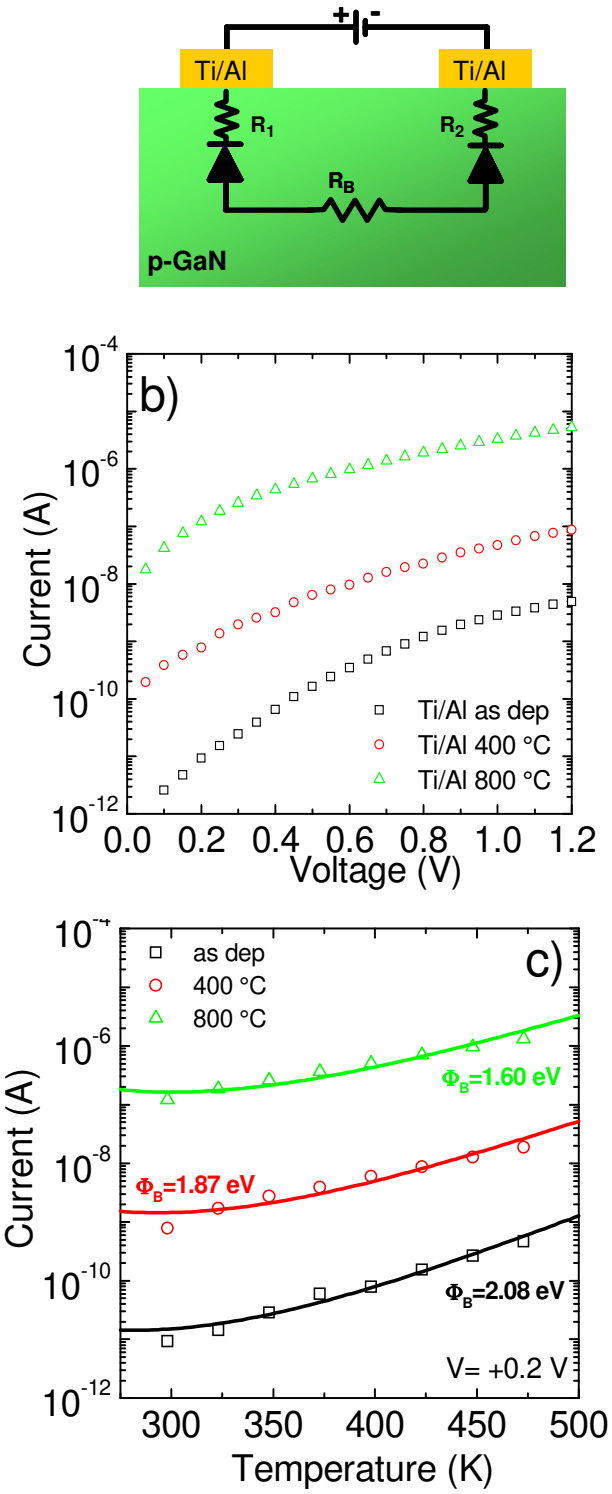

Fig. 11: (a) Schematic cross section of the "back-to-back" test-patterns used to determine the metal/p-GaN barrier height; (b) I-V characteristics acquired on the "back-to-back" structures for the as deposited sample and for the samples annealed at 400 °C and 800 °C; (c) Temperature dependence of the current in the three samples. The continuous lines are the fit of the experimental data obtained by means of the TFE theory, from which the barrier height values could be determined.

The temperature dependence of the I-V measurements, acquired in the back-to-back structures in the temperature range 300-475K, allowed us to get information on the mechanism ruling current transport at the metal/p-GaN interface. In Fig. 11c the temperature dependence of the current acquired at bias of +0.2 V is shown for all three samples. Clearly, an increase in the current with the increasing the measurement temperature is observed. In particular, the experimental data could be fitted using the expression of the reverse current predicted by the Thermionic Field Emission (TFE) model:

$$I_{TFE} = I_S \exp\left[\frac{qV}{kT} - \frac{qV}{E_{00}\coth\left(\frac{E_{00}}{kT}\right)}\right] \tag{2}$$

with $$I_S = \frac{A_c A^* T\sqrt{\pi E_{00}}}{k} \cdot \sqrt{q(V - V_n) + \frac{q\Phi_B}{\cosh^2\left(\frac{E_{00}}{kT}\right)}} \exp\left(-\frac{q\Phi_B}{E_{00}\coth\left(\frac{E_{00}}{kT}\right)}\right), \tag{3}$$

and $$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_A}{m^* \varepsilon}} \tag{4}$$

From the fits of the experimental data (reported as continuous lines in Fig. 11c), the value of Φ_B has been determined for the three cases. The highest barrier height value (Φ_B = 2.08 eV) has been obtained for the as deposited p-GaN/Ti/Al interface. This result is consistent with the theoretical value and with other results reported in literature for Ti/p-GaN interface [59,71]. On the other hand, the value of Φ_B decreases down to 1.87 eV and 1.60 eV, when the annealing temperature is increase to 400 °C and 800 °C, respectively. Moreover in p-GaN/AlGaN/GaN heterostructure, the reduction

of the Schottky barrier height at the metal/p-GaN gate enhances the tunneling of holes through the barrier. Then, as highlighted by Hwang *et al.* [29], the enhancement of holes injection leads not only to a negative shift of the V_{th} and, but also to an increase in the leakage current in p-GaN HEMT. Hence, it is reasonable correlate the electrical degradation of our p-GaN HEMT with the strong decrease in the metal/p-GaN Schottky barrier height observed after annealing treatment.

The structural modification of the metal/p-GaN interface induced by the thermal annealing were monitored by cross section TEM analysis. Fig. 12 reports the cross section TEM micrograph of the p-GaN/Ti/Al structure annealed at 800 °C. Clearly, in such a metal bilayer Ti reacts with Al to form a $TiAl_3$ phase [72]. Moreover, a part of Al does not react with Ti, but it diffuses towards the interface. The result is an inhomogeneous interface, with the presence of Al or $TiAl_3$ in contact with the p-GaN.

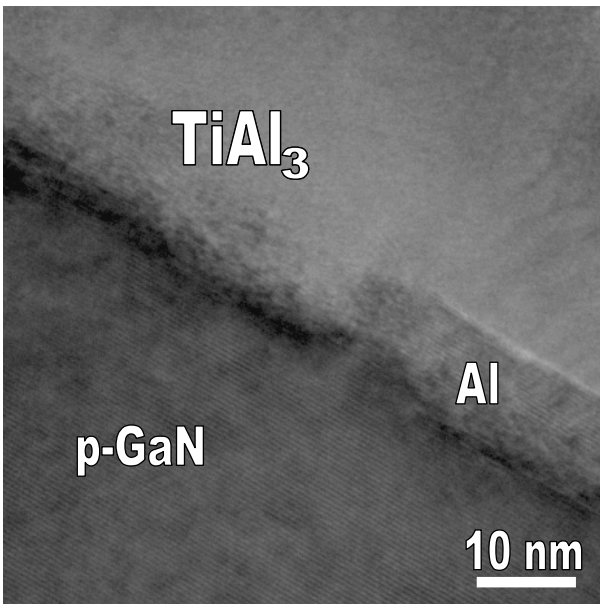

Fig. 12: Cross section TEM micrograph of the p-GaN/Ti/Al interface annealed at 800 °C.

The band structure of the p-GaN/AlGaN/GaN heterostructures, with a metal/p-GaN Schottky barrier of 2.08 eV and 1.60 eV, has been simulated for a gate bias condition of +4 V (see Fig. 13). From these calculations, sheet carrier density values of 4.21×10^{12} cm^{-2} and 5.69×10^{12} cm^{-2} have

been obtained for the as deposited and annealed sample, respectively. Hence, the annealed structure requires a lower (more negative) gate voltage to fully deplete the 2DEG. In addition, at V_G=+4 V the holes depleted from the p-GaN surface are more easily injected at the p-GaN/AlGaN interface in the sample with lower barrier height. This latter can be deduced from the energy difference between the valence band and the quasi-Fermi level for holes. Moreover, at the AlGaN/GaN interface, a high concentration of electrons is detected, due to the presence of the 2DEG. Then, by increasing the positive gate bias, electrons of the channel can be injected over the AlGaN, into the p-GaN. Hence, a higher metal/p-GaN Schottky barrier is useful to obtain a wider depletion region and, hence, reduce the gate current.

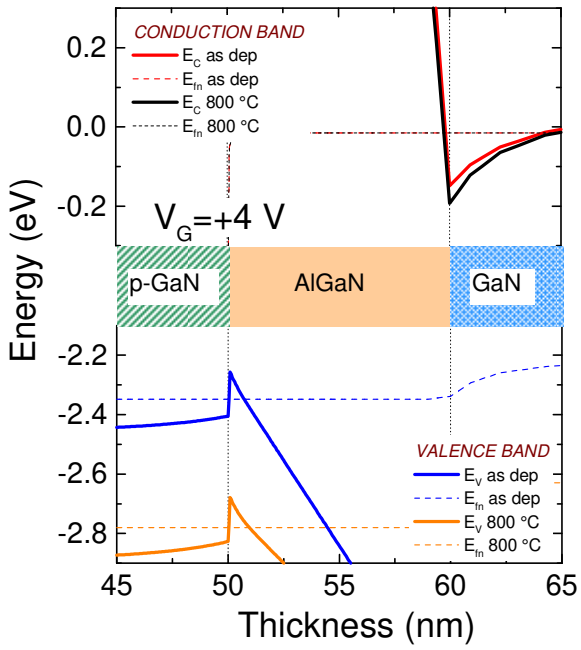

Fig. 13: Magnification of the conduction band and of the valence band for the investigated p-GaN/AlGaN/GaN heterostructures considering annealed (Φ_B = 1.6 eV) and as deposited (Φ_B = 2.08 eV) Ti/Al gate contacts.

3. Recent alternative approaches for normally-off HEMTs with p-GaN

As already specified in section 2.2, one of the critical processing steps for the fabrication of normally-off HEMTs with p-GaN gate is the selective removal of the p-GaN layer by plasma etch.

This process, in fact, can be rather difficult to control, and the plasma-induced damage of the AlGaN surface can lead to a degradation of the electrical properties of the 2DEG in the device access regions. For that reason, the scientific community is also exploring alternative routes to fabricate such devices, which do not involve the dry etch of the p-GaN.

The most straightforward alternative approach to the p-GaN etch is obviously represented by the selective epitaxial growth of p-GaN in localized regions. However, different parameters could impact on the properties of the grown layer, such as the nature and the geometry of the hard mask, [73,74], the growth temperature, [75,76], and the reactor pressure [77]. After the first attempts of selective area growth (SAG) of GaN [78,79], this process has been proposed for different purposes, such as for the fabrication of non-alloyed Ohmic contacts [80,81], recessed gate MOS-HEMT structures [82,83], or innovative optoelectronics nanostructures (light emission diodes, laser diodes, etc) [84,85].

In this context, Yiuliang *et al.* [86] recently reported on the fabrication of a device employing the selective area growth (SAG) of a p-GaN layer below the gate region. For this purpose, a 100nm thick silicon oxide (SiO_2) hard mask, patterned by photolithography and wet etch, has been used for the selective growth of the Mg-doped p-GaN layer by MOCVD at 1000°C. Although the re-grown p-GaN layers exhibited a smooth morphology, their cross-sectional profile was not sharp, probably due to a non-uniform growth along the side-walls of the hard mask. The fabricated devices showed a positive shift of the threshold voltage V_{th}, which increased from the value of -3.95 V measured in the reference Schottky gate device to -0.37V in the SAG HEMT. Obviously, a further optimization of the SAG process is still required to achieve a larger positive shift of the V_{th}. Additionally, a more appropriate choice of the hard mask can be important to guarantee the uniformity of dopant incorporation and thickness in the re-grown layer [87]. These aspects will be crucial to understand the real feasibility of the selective growth process for practical devices applications.

Another very interesting approach has been recently published by Hao *et al.* [88], who proposed to replace the p-GaN etching process with an hydrogen plasma surface treatment (Fig. 14c). In fact,

hydrogen atoms can produce a hole compensation mechanism in the p-type Mg-doped GaN, due to the formation of Mg-H neutral complexes, which passivate the Mg-acceptors in the p-type GaN layer [36]. In this way the hydrogen surface treatment of the access regions modifies the properties of the cap layer, and the conduction band is locally pulled again below the Fermi level, restoring the 2DEG at AlGaN/GaN interface in the access regions. The devices fabricated with this approach exhibited a threshold voltage V_{th}=+1.75V, and a current density of 188mA/mm at the maximum gate voltage swing of +6V.

In Fig. 14 the schematic cross sections of normally-off p-GaN HEMTs standard p-GaN dry etching process (Fig. 14a) is reported together with the two aforementioned alternative approaches using the SAG of the p-GaN (Fig. 14b) and the hydrogen plasma surface treatment (Fig. 14c).

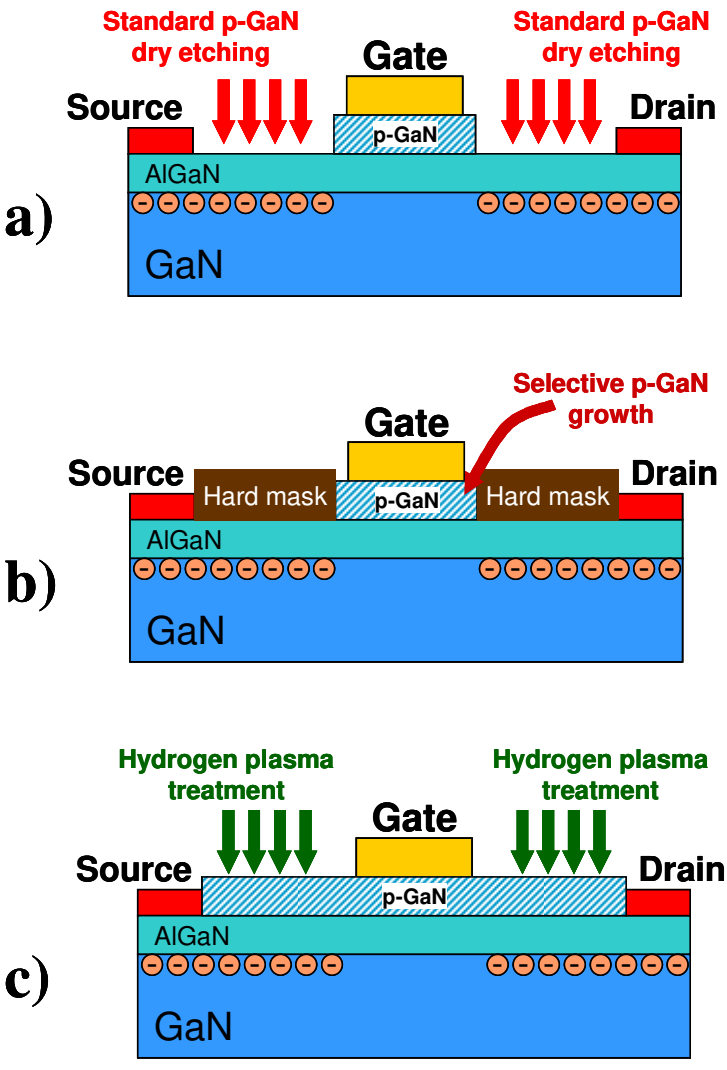

Fig. 14: Schematic cross section of normally-off p-GaN HEMTs fabricated with different process, i.e., (a) standard p-GaN dry etching process, (b) selective area growth (SAG) of p-GaN and (c) hydrogen plasma surface treatment for local Mg deactivation.

Besides the aforementioned methods, it is worth mentioning that also other processes aimed to replace the p-GaN gate with other semiconductors material are under investigation. One of the most promising consists in the replacement of the p-GaN cap layer with another thin p-type doped semiconductor with favorable band gap and band offset with respect to GaN. In this context, nickel oxide (NiO) has a wide band gap (4eV) and a high permittivity (11.9) [89], thus making it a promising insulator for GaN-based devices. In fact, NiO has been successfully tested as dielectric material in HEMT structure to suppress the gate leakage current [90,91]. However, under certain conditions NiO can behave also as p-type semiconductor and, hence, play the same role of the p-GaN cap if grown onto an AlGaN/GaN heterostructure. As a matter of fact, some authors reported on the possibility to synthesize p-type semiconducting NiO_x films by cheap methods (e.g., oxidation of nickel films) and to integrate this process in the fabrication of normally-off AlGaN/GaN HEMTs with a p-type NiO gate [19,20,92]. However, the post deposition annealing conditions to obtain p-type conductivity of the synthesized films can be rather difficult to control [93] and the used oxidizing annealing can have a detrimental effect of the properties of the 2DEG [17]. For that reason, these processes are still under investigation to understand the real possibility to integrate in the fabrication flow-chart of GaN-based HEMTs.

Clearly, although the definition of the p-GaN gate by selective plasma etch processes presents some inconvenience, it still remains the unique industrialized approach used for the fabrication of normally-off HEMT.

4. Summary

In this paper, some of the most important technological issues related to the fabrication of normally-off p-GaN HEMTs have been reviewed. First, the device operation principle was illustrated, pointing out the importance of the heterostructures parameters for an efficient depletion of the 2DEG. In particular, using thin AlGaN barrier layers (~10nm) with an Al molar fraction of 26% gives a good compromise between the threshold voltage and the 2DEG concentration. For the selective etch of the p-GaN, low power Cl_2-based processes, at a low etch rate, are indicated to define the p-GaN gate region, without significant alteration of the surface morphology and 2DEG properties in the access regions. One of the most critical parts of the device is the p-GaN layer and its gate electrode. In this respect, the advantage to use Schottky over Ohmic contacts solutions has been pointed out, where low work-function metals (e.g., Ti-based systems) are more suitable to increase the value of the Schottky barrier height. However, particular attention must be done on the thermal stability of the metal gate upon annealing, since thermal reactions can lead to a decrease in the Schottky barrier height and, hence, to an increase in the leakage current and a lowering of the V_{th}. In this sense, “gate last” processes (i.e., in which the metal gate is fabricated at the end of the flow-chart and not subjected to significant thermal budged) or refractory metals should be preferred to avoid these undesired effects. Finally, also novel approaches based on the selective re-growth of the p-GaN gate or the local deactivation of the Mg-dopant by hydrogen plasma processes have been recently proposed in literature. However, further optimization are still required to obtain a reliable behavior of the fabricated devices.

In conclusion, the results summarized in this review paper provide the general trends for design rules and processing conditions to fabricate AlGaN/GaN normally-off HEMT with a p-GaN gate and, hence, can be useful for the GaN devices community.

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