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Elimination of carbon vacancies in 4H-SiC employing thermodynamic equilibrium conditions at moderate temperatures

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ABSTRACT

The carbon vacancy (V_C) is a major point defect in high-purity 4H-SiC epitaxial layers limiting the minority charge carrier lifetime. In layers grown by chemical vapor deposition techniques, the V_C concentration is typically in the range of 10^{12} cm^{-3}, and after device processing at temperatures approaching 2000 °C, it can be enhanced by several orders of magnitude. In the present study, both as-grown layers and a high-temperature processed one have been annealed at 1500 °C and the V_C concentration is demonstrated to be strongly reduced, exhibiting a value of only a few times 10^{11} cm^{-3} as determined by deep-level transient spectroscopy measurements. The value is reached already after annealing times on the order of 1 h and is evidenced to reflect thermodynamic equilibrium under C-rich ambient conditions. The physical processes controlling the kinetics for establishment of the V_C equilibrium are estimated to have an activation energy below ~3 eV and both in-diffusion of carbon interstitials and out-diffusion of V_C's are discussed as candidates. This concept of V_C elimination is flexible and readily integrated in a materials and device processing sequence.

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Silicon carbide (SiC) and in particular, the 4H polytype acquire a rapidly growing impact as a superior material for advanced power electronic applications. For instance, a 4H-SiC PiN diode with a breakdown voltage of ∼27 kV was recently reported by Kaji *et al.*[1] using a 270 μm thick epitaxial layer with a 1050 μm long space-modulated junction termination. However, for such high-voltage bipolar devices, the presence of electrically active point defects is a serious obstacle since they strongly limit the possibility to obtain charge carrier modulation and low on-state voltages. Therefore, special measures are required to reduce the defect concentration for enhancement of the charge carrier lifetime to values well above 10 μs. The carbon vacancy (V_C) was recently found to be the origin of the so-called $Z_{1/2}$ and EH_7 deep energy levels,[2] which are the main carrier lifetime killer in 4H-SiC.[3–5] The $Z_{1/2}$ level was ascribed to the double negative acceptor state, V_C(2-/0), and EH_7 to the single donor state, V_C(0/+).

In state-of-the-art as-grown epitaxial layers, [V_C] (brackets denote concentration) is in the 10^{12} cm^{-3} range which is too high to obtain a charge carrier lifetime in excess of ∼5 μs. Currently, two different procedures are commonly pursued to reduce the [V_C]: (i) thermal oxidation of the Si-terminated surface of the epi-layers,[6–10] and (ii) near surface ion implantation followed by high temperature annealing.[11,12] Both (i) and (ii) utilize injection of interstitial carbon atoms (C_i's) generated in the near surface region and subsequent annihilation of the V_C's in the epi-layer "bulk".

In addition to the existence of V_C's in as-grown layers, also V_C formation during high-temperature device processing can be challenging. Actually, annealing temperatures above ∼1800 °C are necessary for sufficient electrical activation of high fluence ion-implanted Al atoms in order to realize low-resistivity p^+ layers.[13] In a recent study, we have investigated the evolution of [V_C] in 4H-SiC epi-layers during isochronal heat treatment from 1600 to 1950 °C (10 min) under thermodynamic equilibrium conditions in C-rich ambient.[14,15] The [V_C] was found to increase rapidly with temperature, and a formation energy (enthalpy) of ∼5.0 eV for V_C was deduced together with an entropy factor of ∼5 k.[14,15] Also recent results from large scale and bandgap error free calculations, based on density-functional-theory (DFT), yield an energy of ∼5.0 eV for the V_C formation under C-rich ambient conditions.[16,17]

In the present study, we show that annealing at moderate temperatures under C-rich thermodynamic equilibrium conditions can reduce the [V_C] in 4H-SiC epi-layers down to the low 10^{11} cm^{-3} range. The equilibrium is reached rather rapidly and both in-diffusion of C_i's from the ambient, followed by recombination with the V_C's in the epi-layer, and out-diffusion of V_C's are likely candidates for the physical processes controlling the kinetics to establish the equilibrium. The annealing procedure is straightforward and may be regarded as superior to those commonly used today for the V_C elimination, (i) and (ii) described previously. Furthermore, it provides the possibility of re-annealing high-temperature processed wafers; the validity of this approach is demonstrated by 1500 °C re-annealing of a sample first heat treated at 1950 °C, leading to a reduction in the [V_C] by almost three orders of magnitude down to the equilibrium value at 1500 °C.

Samples with a size of 5 × 7 mm^2 were cut by laser from an n-type 100 mm diameter 4H-SiC epitaxial wafer purchased from Cree, Inc. The epi-layer was grown by chemical vapor deposition (CVD) 4° off the c-

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axis on top of the (0001) Si surface of a highly doped substrate ($\sim 10^{18}$ cm^{-3}). The thickness of the epi-layer was $\sim 10\,\mu$m and nitrogen was used as the n-type dopant. The net carrier concentration was $\sim 1 \times 10^{15}$ cm^{-3} as determined by capacitance-voltage (CV) measurements undertaken at room temperature (RT) with a 1 MHz probe frequency. Two samples were subjected to heat treatment at 1500 °C for 40 min and 3 h, respectively, in high-purity Ar ambient employing a tube furnace. A third sample underwent high temperature treatment at 1950 °C for 3 min in high-purity Ar ambient using an inductively heated furnace and was then cooled down rapidly (quenched) with an almost exponential temperature decrease having a time constant of $\sim$50 s. This sample was subsequently re-annealed at 1500 °C for 3 h in the tube furnace under high-purity Ar ambient. Prior to all the heat treatments, the samples were protected by a pyrolyzed resist film (C-cap) after native oxide etching, where the pyrolysis was performed in forming gas at 900 °C for $\sim$5 min. The C-cap was removed after the annealing treatments by dry thermal oxidation at 850 °C for $\sim$15 min.[18]

After a standard cleaning procedure, circular Schottky barrier diodes (SBD) with a diameter of 1 mm were formed by electron beam evaporation of Ni on top of the epi-layer surface. Silver paste was applied on the back side of the samples to form an Ohmic contact. Deep level transient spectroscopy (DLTS) and defect concentration-versus-depth profiling measurements were employed for characterizing the samples using a refined version of the setup described in Ref. 19. The [V_C] was monitored via the V_C(2-/0) level (also known as the $Z_{1/2}$ level) located at $\sim$0.7 eV below the conduction band edge and having a peak position of $\sim$285 K in DLTS spectra with a rate window of (640 ms)$^{-1}$.

As depicted in Fig. 1, [V_C] decreases from $\sim 4 \times 10^{12}$ cm^{-3} in the as-grown epi-layers to $\sim 2 \times 10^{11}$ cm^{-3} after annealing at 1500 °C for 40 min. Fig. 1 reveals also that increasing the annealing duration to 3 h does not influence the [V_C] which remains in the low 10^{11} cm^{-3} range. This implies strongly that [V_C] has reached thermodynamic equilibrium and indeed, profiling results show also a uniform concentration-versus-depth distribution of V_C up to the maximum depth probed ($\sim 3\,\mu$m), as illustrated in Fig. 2. As discussed in Refs. 14 and 15, the V_C formation at high temperatures under C-rich ambient conditions appears to be controlled by atomistic processes in the epi-layer "bulk" rather than Schottky formation at the surface with subsequent in-diffusion of V_C. For the V_C reduction and equilibration at moderate temperatures, two basic physical processes can occur: in-diffusion of C_i from the C-rich ambient followed by annihilation with V_C ($C_i + V_C \rightarrow \phi$) and/or out-diffusion of V_C towards the surface. The uniformity of the V_C concentration-versus-depth profiles in Fig. 2, which is expected for equilibrium conditions, does not exclude (nor favor) any of these two physical processes. The maximum probed depth of $\sim 3\,\mu$m below the surface is rather shallow and limited by the net doping concentration of the epi-layer in combination with the maximum applicable reverse bias voltage of the experimental setup. At larger depths the [V_C] may increase; however, if we assume, as a first approximation, that the whole epi-layer ($\sim 10\,\mu$m) is equilibrated within 40 min at 1500 °C, a diffusivity of $\geq 5 \times 10^{-10}$ cm^2/s is required for the prevailing species. Theoretically, C_i is found to be highly mobile with a migration energy of only $\sim$1 eV, or even less for the positive and neutral charge states,[20] and its diffusivity at 1500 °C readily exceeds 5×10^{-10} cm^2/s by several orders of magnitude. In contrast, V_C is theoretically predicted to be much

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less mobile with a migration energy of ~3.5 eV in the neutral charge state (which is the expected one in our samples during the annealing at 1500 °C). Accordingly, these theoretical data support C_i injection as the dominant physical process provided that diffusion barriers at the surface are below ~1 eV. On the other hand, only a slightly lower V_C migration barrier of ~3 eV together with a pre-exponential factor of 1 cm^2/s yields a diffusivity in the 10^{-9} cm^2/s range at 1500 °C. Hence, V_C may also be sufficiently mobile and its impact on the equilibration process cannot be ruled out. Moreover, prior to the 1500 °C anneal, the samples have been subjected to higher temperatures under C-rich conditions, during the growth and/or the post-growth processing, and the total carbon content in the samples is probably above its equilibrium value at 1500 °C. Accordingly, in-diffusion of C_i is expected to be suppressed, indicating that V_C out-diffusion plays an important role. Further studies need, indeed, to be pursued in order to identify the dominant physical process, and especially, accurate experimental data for the migration of V_C and C_i are highly desirable.

In Fig. 3, experimental data for the equilibrium concentration of V_C under C-rich ambient conditions are compiled from the present study and from Refs. 14 and 15, covering temperatures from 1500 to 1950 °C. The data obey closely the relation

$$[V_C] = N_{C-sites}\ exp\left(\frac{\Delta S}{k}\right)\ exp\left(\frac{\Delta H_{Form}}{kT}\right) \tag{1}$$

with the concentration of C-sites in the SiC lattice, $N_{C-sites}$, put equal to 5×10^{22} cm^{-3}, the increase in crystal entropy associated with the V_C formation, ΔS, equal to $\sim 5k$, and the formation enthalpy of V_C, ΔH_{Form}, equal to 4.8 eV. In Eq. (1), k is the Boltzmann's constant and T is the absolute annealing temperature. Within the experimental accuracy, these values deduced for ΔH_{Form} and ΔS by least-square fitting are in full accord with those reported previously using a smaller set of data.[14,15]

Fig. 3 illustrates not only how the $[V_C]_{Equilibrium}$ depends on temperature but also suggests how it can be tailored by post-growth and/or post-processing annealing. The tailoring requires, however, sufficiently rapid kinetics for the establishment of $[V_C]_{Equilibrium}$ in order to be truly applicable for materials and device processing. As indicated by Fig. 1 and as discussed above, at 1500 °C the $[V_C]_{Equilibrium}$ occurs after an annealing duration of less than 1 h for as-grown epi-layers, and also the applicability of post-processing annealing (or re-annealing) to tailor the $[V_C]$ is shown by the results in Fig. 4. After treatment at 1950 °C for 3 min, which is a typical post-implant anneal of high-fluence Al ion implanted layers to accomplish efficient electrical activation,[21] the $[V_C]$ exhibits a value of $\sim 2 \times 10^{14}$ cm^{-3}. This corresponds to the DLTS peak amplitude of ~0.16 for the V_C(2-/0) level in Fig. 4. Subsequent annealing of the sample at 1500 °C for 3 h reduces the V_C(2-/0) peak amplitude by almost three orders of magnitude, close to the detection limit of the DLTS measurements. The V_C concentration extracted after the re-annealing is in the low 10^{11} cm^{-3} range, and as shown in Fig. 1, it is identical to the $[V_C]_{Equilibrium}$ obtained after the 1500 °C annealing of the as-grown epi-layers, accounting for the experimental accuracy.

Hence, annealing at 1500 °C under C-rich conditions emerges as a viable and alternative procedure to (i) thermal oxidation and (ii) post-implant annealing of near-surface ion-implanted layers for the elimination of V_C's and enhancement of the charge carrier lifetime. The dominant physical process controlling the annihilation kinetics of V_C may be the same as in (i) and (ii), i.e., injection of highly mobile C_i's recombining with V_C's. However, the resulting [V_C] after the treatments (i) and (ii) is a non-equilibrium one and the V_C concentration may increase during subsequent processing. In contrast, the equilibrium annealing procedure provides a possibility to reduce the [V_C] after high-temperature processing.

Finally, it should be noted that annealing (and re-annealing) below 1500 °C can be even more efficient for the V_C elimination, see Fig. 3, but a more extended duration to reach thermodynamic equilibrium is needed. Data presented in Ref. 22 indicate that annealing times in excess of 40 min are required to establish equilibrium at 1400 °C.

In summary, annealing of 4H-SiC epi-layers at the moderate temperature of 1500 °C under C-rich conditions is shown to reduce the [V_C] to the low 10^{11} cm^{-3} range. This holds for both as-grown layers and high-temperature processed ones with a relative reduction in the [V_C] by a factor of ~10 and ~10^3, respectively. The [V_C] obtained after 1500 °C annealing is evidenced to reflect thermodynamic equilibrium and it is established within a duration on the order of 1 h. This indicates an activation energy of ~3 eV, or less, for the physical process governing the equilibration of [V_C]. Both injection of C_i's leading to recombination with V_C's and out-diffusion of V_C's to the surface are discussed as candidates as the dominant physical process, although theoretical migration energy values favor the former one. Technologically, annealing at moderate temperatures appears as a viable and straightforward concept for V_C elimination. In particular, the procedure is readily integrated in a materials and device process flow, and it can be regarded as superior compared to those commonly used today for V_C elimination.

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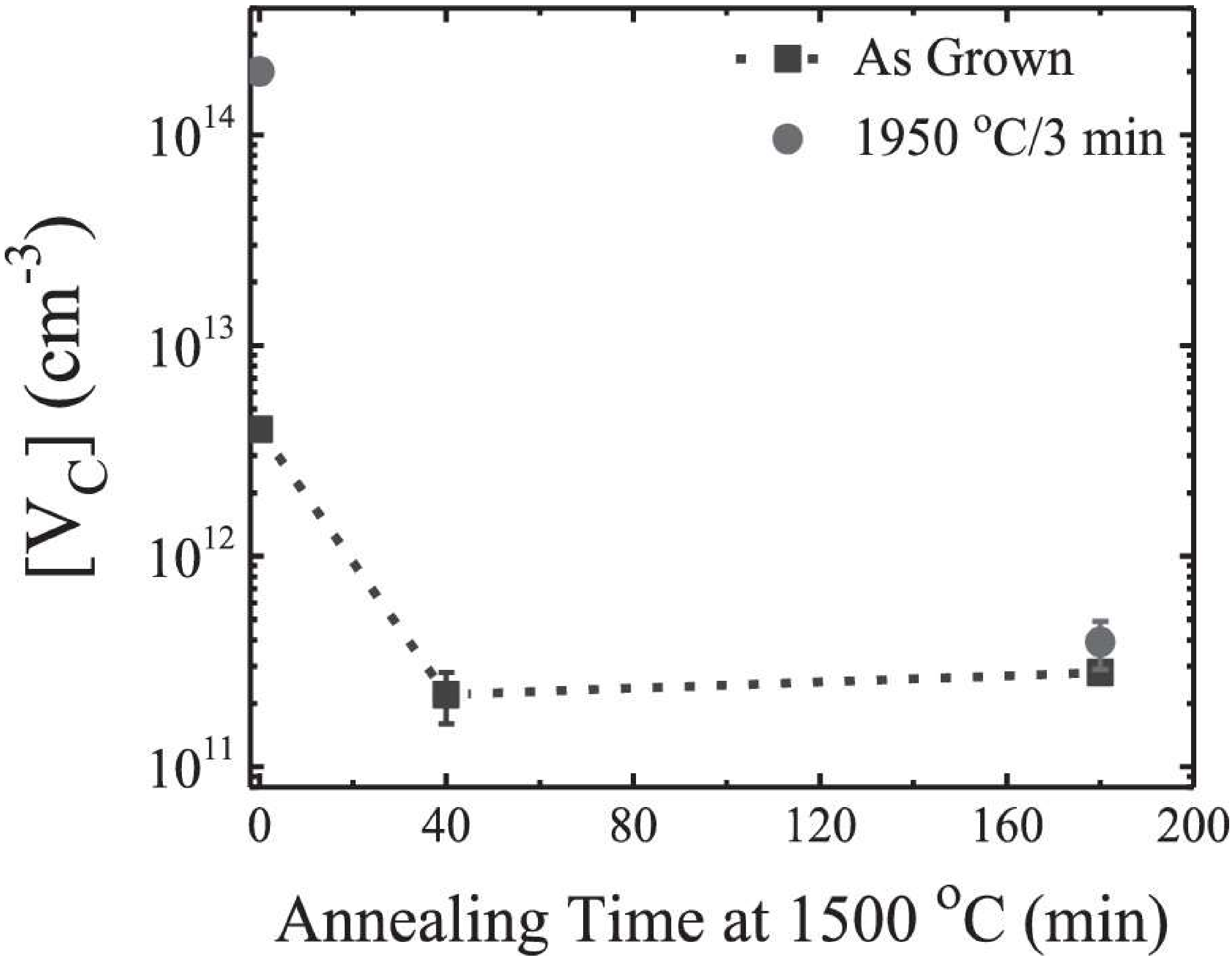

FIG. 1. V_C concentration versus annealing time at 1500 °C under C-rich ambient conditions for as-grown 4H-SiC epi-layers. Data for a sample processed first at 1950 °C (3 min) and then re-annealed at 1500 °C for 3 h are also included.

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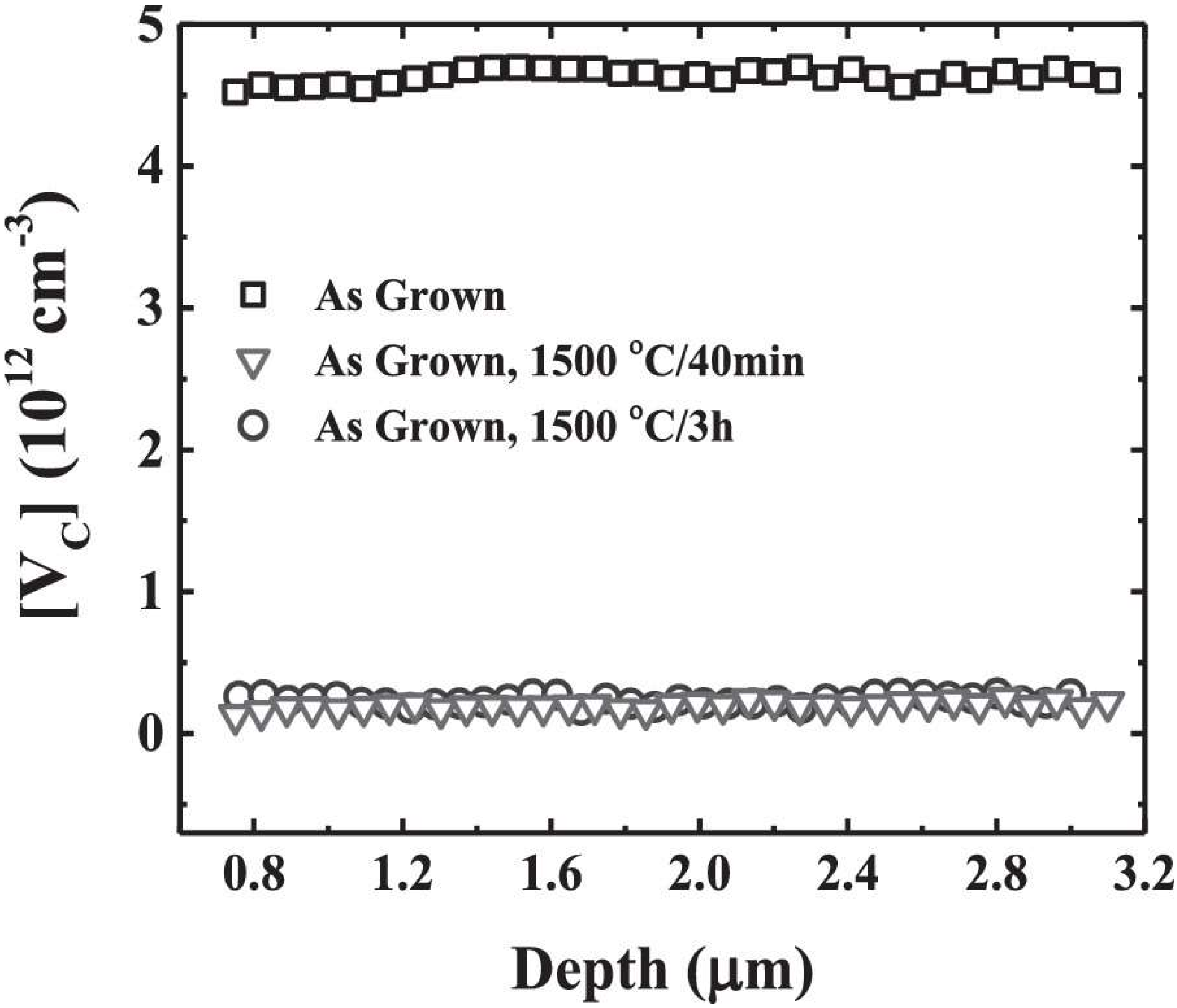

FIG. 2. Concentration-versus-depth profiles of V_C in an as grown 4H-SiC epi-layer and in as-grown layers subsequently annealed at 1500 °C for 40 min and 3 h.

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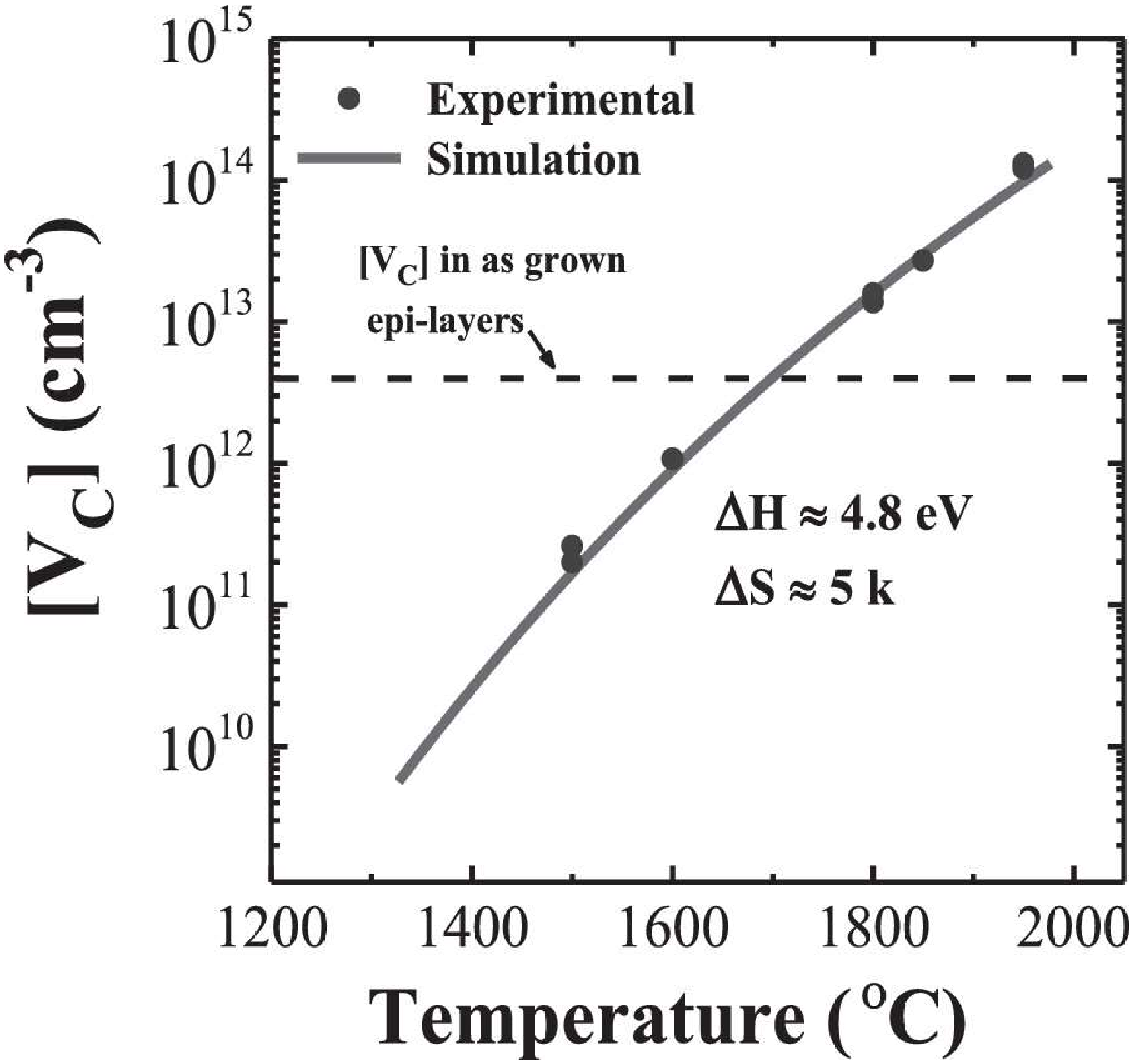

FIG. 3. Calculated V_C concentration as a function of temperature under thermodynamic equilibrium conditions using $\Delta H_{Form} = 4.8\ eV$ and $\Delta S = 5\ k$, together with experimental data compiled from the present study and Refs. 14 and 15.

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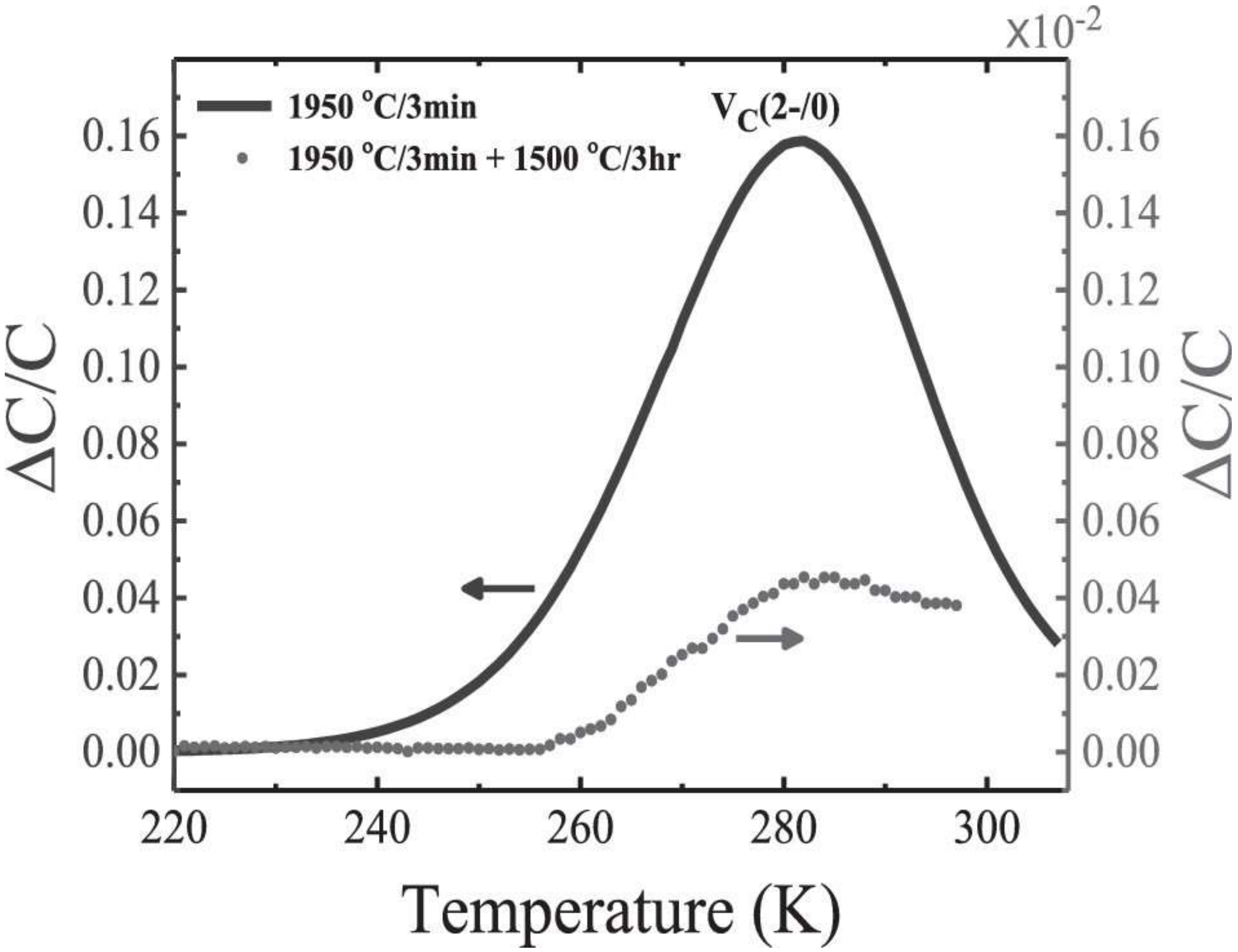

FIG. 4. DLTS spectra of V_C(2-/0) in an n-type 4H-SiC epitaxial layer subjected to a high temperature treatment at 1950 °C for 3 min (left y-axis) and then re-annealed at 1500 °C for 3 h (right y-axis). (DLTS rate window = (640 ms)$^{-1}$.)