3C-SiC carbonization optimization and void reduction on misoriented Si substrates: from research to production scale reactors

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Abstract
In this work we study how to optimize the carbonization process in order to deposit cubic SiC (3C-SiC) on misoriented Si substrates. The carbonization process is a key step to obtain device-quality layers and to partially release the strain due to the lattice mismatch between the substrate and the thin 3C-SiC film. One of the common problems in SiC/Si epitaxy is the presence of interfacial voids that can degrade the structural quality of the deposited film and the electrical properties in vertical devices.
The carbonization optimization requires a careful control of several parameters, in particular temperature, precursor flows, heating ramps. Precise tailoring of this process on a production reactor with the understating of all the involved variables would requires a huge effort in terms of time and money, so it is desirable to perform part of this work on a smaller scale research reactor, more versatile and economically viable.
Starting from a baseline process for 3C-SiC power devices on 100mm Si, already developed on a production reactor, we used a small research reactor to investigate how the thermal heating profile during the carbonization ramp influences the void density on the Si substrate. We have also studied how the introduction of silane during the carbonization ramp can effectively suppress void formation.
After having obtained a comprehensive understanding of the variables involved in the process, the key ideas were successfully transferred to the production reactor, with a significant reduction of interfacial voids.

Introduction
Thanks to its outstanding physical properties, SiC is a promising material for the realization of power switches [1,2]. SiC can crystallize in a large number of polytypes but the cubic form can be epitaxially grown on Si, enabling the fabrication of diodes and Metal-Oxide Field Effect Transistors (MOSFETs) on conventional Si wafers rather than using expensive bulk SiC substrates [3,4]. This reduces the cost by a factor up to 20 and opens up the possibility of fabricating SiC devices at similar costs to those made on Si.
Many problems arise during SiC/Si heteroepitaxy due to the large lattice and thermal expansion coefficient mismatches: amongst them antiphase domains, wafer bending, extended defect generation and voids at the interface [5]. Antiphase domains are given by the nucleation of a polar material (SiC) onto a non-polar substrate (Si) and the boundary between two adjacent domains may act as an active center that degrades electrical properties of the material. The growth on misoriented Si (001) substrate (4°off) permits to avoid the problem of antiphase domains generation, thanks to an ordered step flow growth. [6,7] Moreover, controlling the height of the steps in the silicon substrate surface through a misoriented substrate, in particular having bi-atomic steps instead of mono-atomic ones, permits to obtain a SiC heteroepitaxy free of anti-phase boundaries. [8,9]
In SiC/Si epitaxy the surface of Si substrate is usually converted to a thin SiC layer by using carbon precursors such as propane, ethylene or ethane [10,11,12]. The carbonization occurs by flowing the C-precursor from room to growth temperature, then pausing several minutes at intermediate carbonization temperature, usually in the range between 1000 and 1150°C. During the second heating step (up to ~1350-1400°C) small voids can form at the SiC/Si interface, which may degrade device performance, hamper the realization of heterojunction bipolar transistors, influence extended defect generation and increase residual strain.
Several groups improved the standard carbonization process by using multistep methods, changing the ramp heating rate and introducing silane with propane in variable concentration during the heating stage. [13, 14, 15, 16, 17, 18]. These procedures result ultimately in the deposition of a so called “low temperature SiC buffer layer”, often 10-200 nm thick, over the carbonization process at low

temperature. The use of buffer layer is very common in lattice mismatched epitaxy (e.g. GaN/sapphire, Ge/Si, InGaAs/InP) and helps to relieve lattice mismatch, to reduce strain and to increase the quality of the thick epitaxial layer [19]. Some of the authors of this paper studied a thick buffer deposition process which permitted to growth thick SiC film on exacly oriented Si substrates, with low strain content [20,21]. The key idea of this process was to control the ramp time in order to avoid the formation of voids and to inject a variable concentration of silane during the temperature ramp from 1100 °C to 1380 °C.

Anvil Semiconductors Ltd [22] has developed a unique technology that enables the growth of device quality 3C-SiC epitaxy on 100mm and 150mm Si wafers, up to 12 microns in thickness, to permit the fabrication of vertical power devices. A lot of effort was devoted towards the development of a proprietary process that minimizes the effect of the mismatches in lattice parameter and thermal coefficient of expansion: a polycrystalline SiC grid is used to divide the wafer into squares small enough to reduce the effect of lattice mismatch and thermal expansion but sufficiently large to fabricate complex devices. Thick (around 10µm) epitaxial layers with acceptable bow have already been demonstrated on 100mm diameter wafers and the process is being migrated onto 150mm diameter wafers.

However, the presence of interfacial voids between SiC and Si still had an impact on layer quality, increase extended defects generation and degrading the performances of some kind of devices.

Anvil Semiconductors Ltd developed its process on a dedicated industrial reactor but it was evident that, in order to suppress void formation, a large number of experiments would have been needed to understand the effect of all the parameters involved, namely carbonization temperature and time, carbon flow, ramp heating time, silane flow and injection temperature during the heating ramp. In order to reduce the costs and to speed up the development, a small Vapor Phase Epitaxy (VPE) research reactor was chosen to reproduce the process already developed on the production reactor and to perform dedicate experiments focused on the study of the carbonization process. A lot of growth runs were thus performed at a fraction of the production cost and time and the variables involved in the carbonization were extensively studied to obtain useful indications on their effect on the final SiC film.

This work summarizes the results obtained on the carbonization process on Si misoriented substrates. We used different thermal ramp rates and shapes to heat the substrate from carbonization temperature to growth temperature. The process was stopped at different stages to study voids formation and evolution over temperature. Moreover, void formation was almost completely eliminated by the introduction of silane during the heating ramp. Although several papers about voids elimination on exacly oriented Si (001) and Si (111) substrate were already published, at the best of authors' knowledge this is the first comprehensive work on void suppression on misoriented Si (001) substrates. These studies were performed on a small research reactor and, after having obtained a comprehensive understanding of the variables involved in the process, the key ideas were successfully transferred to the production reactor which resulted in the elimination of interfacial voids.

Experimental

The 3C-SiC layers were deposited in two different horizontal hot-wall VPE reactors, on (001) Si substrates misoriented 4° off towards the (110) direction. The precursors used were SiH_4 and C_2H_4, diluted in ultrapure H_2 as carrier gas. Heating was obtained by radio-frequency induction in both cases. Since the precursor flow needed for carbonization and for SiC film growth has a very different range, two different ethylene gas lines were used, with independent mass flow controllers.

The research reactor is an home-made equipment with a graphite hot-wall growth chamber of the dimension of about 1.2x3x10 cm^3 (height x width x length). In this reactor we used substrates chips of the dimension of approximately 1.5 x 3 cm. The reactor has a custom software control handled by a Programmable Logic Computer (PLC) that can be completely customized depending on the particular needs, and is capable of running an automatic process with user-defined specification, permitting to avoid operator-dependent variables.

The production scale reactor is an Epigress VP508GFR located in Norstel AB [23], Norrkoping (Sweden), designed to load 100mm Si wafer and adapted for 150 mm wafers.

The baseline process developed on the production scale reactor by Anvil Semiconductors Ltd was adapted to the research reactor by calibrating the flows and the deposition temperatures, taking into consideration the scale factors between the two equipments. The standard process was then further enhanced by varying several parameters, as it will be described in the following sections.
Because of the commercial nature of the process for the power-device production and the non disclosure agreements between the production, research facilities and Anvil Semiconductors Ltd, the detailed growth conditions of the production reactor cannot be described in this work. Only the growth conditions for the research reactor will be given, so all the subsequent flows, partial pressures, precursor ratios and growth details will be referred to the research reactor.
Prior to growth, the Si wafers were etched in HF:H_2O (1:20) to remove the native oxide and were immediately loaded into the growth reactor.
The whole process is performed at 200 mbar with 4000 sccm H_2 flow. The carbonization begins with a heating ramp from room temperature to 1000 °C under a 20 sccm ethylene flow, that will remain constant until the thick 3C-SiC film growth at high temperature begins. The duration of this first ramp is about 15 minutes. After this step the temperature is held at 1000 °C for 10 minutes. 3C-SiC film growth is then performed at higher temperature, around 1380 °C: the transition from low temperature carbonization (1000 °C) to high temperature is one of the most critical step of the process. Interfacial voids at the SiC/Si interface generate at some point during this stage and the carbonization must provide an optimum SiC layer in order to nucleate a monocrystalline film once the temperature reaches the growth regime. The ethylene flow, the initial heating ramp to the carbonization temperature and the carbonization temperature itself of 1000 °C were chosen after an initial optimization of the parameters and were not changed during the subsequent experiments.
In our previous works on the SiC buffer optimization on exactly oriented Si substrates we observed that the ramp time during the heat from carbonization temperature to the growth temperature has a great influence on voids generation[20]. We thus applied the same idea to the process on misoriented substrates, even if the carbonization temperatures were different between the two cases.
In order to understand how the heating process between 1000 °C and 1380 °C influences void generation we investigated different heating ramp shapes: linear (with two different lengths, 600 and 2000 seconds), exponential and inverse exponential (both lasting 2000 seconds). The temperature versus time for the used ramps are reported in Fig. 1. The two exponential ramps were in the form $T=A+B\exp^{mt}$ and $T=A+B\exp^{-mt}$ where t is the time, T the temperature and A, B, m are reported in Table 1. The exponential curves were fitted with a 4^{th} order polynomial expression in order to implement them in the PLC. The reactor setpoint was then varied accordingly over time and the actual reactor temperature correctly followed the setpoint.
To figure out if there is a critical temperature at which voids are preferentially generated, we stopped the growth at different temperatures during the heat up for each of the adopted ramps: the carbonization was thus interrupted at 1150 °C, 1250°C, 1300°C and 1325 °C and the sample was cooled in Ar atmosphere to avoid unwanted generation of void due to H_2 etching during the cooldown.

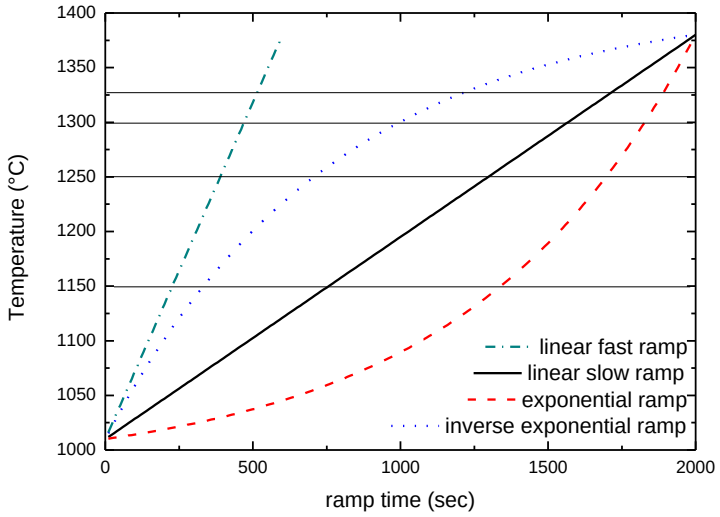


Fig. 1: different heating ramps used to study the carbonization. The horizontal lines are placed at the temperatures at which the ramp was stopped for the voids observation.

	A	**B**	**m**
Exponential ramp	980	30	0,012951
Inverse exponential ramp	1410	400	0,016226

Table 1: coefficients used for the exponential heating ramps.

We observed that cooling the sample in Ar right after the end of the carbonization process, from 1380 °C to room temperature, gave irreproducible results in terms of void density from run to run so a SiC film, about 1 μm thick, was grown after the different carbonization processes to protect the surface. This was probably due to some etching effect during the initial phase of the cooldown. For the SiC film deposition we used Si / C = 1.4 in the gas phase, because in this reactor the Si cracking efficiency is low.
In order to study how the introduction of SiH_4 suppresses voids formation, we injected SiH_4 with different flow rates (0.1 – 0.3 sccm) during the heating ramp, starting at different temperatures (1000, 1200, 1250, 1300, 1325 °C).
The resulting layers were observed by means of an optical microscope and with a Zeiss Auriga Compact Scanning Electron Microscope (SEM) to evaluate void density. The samples with the SiC overlayer were cut and observed in cross section at the SEM.
X-Ray Diffraction Measurements (XRD) were performed with a Panalytical Empyrean diffractometer equipped with a hybrid monochromator consisting of a parabolic X-ray mirror and a two-bounce Ge(220) and a symmetric three-bounce Ge(220) analyzer.

Results and discussion

The growth conditions for the SiC carbonization on misoriented Si (001) substrates were found to be different from the one used on exactly oriented (001) substrate, due to the different surface energy and mobility of adatoms given by the presence of steps: we initially tried to utilize the same buffer process we developed on exactly oriented substrate[20] but the result was an ineffective suppression of interfacial voids and a low quality epitaxial SiC film, with high surface roughness and hazy appearance.
In order to develop the research process on misoriented Si substrates we thus started from the baseline process for 3C-SiC power devices on 4'' Si, already developed on the production reactor.

The initial carbonization process from 1000 °C to 1380 °C used a linear ramp lasting 600 sec (“fast ramp”), and resulted in a lot of voids observed at the SiC/Si interface. The SiC layer looked also quite hazy at the naked eye.
The carbonization was initially checked right after its end, by cooling the sample after the 10 minutes hold at 1000 °C in ethane flow: the resulting surface, as observed at SEM, was completely featureless, indicating that no voids are formed at 1000 °C.
The optical microscope analsys revealed an almost featureless surface up to 1250 °C for all the ramps shapes considered. SEM investigations were although useful to spot the presence of tiny voids also at 1150 °C, with dimensions of about 100-150 nm. Fig. 2 shows the evolution of the voids from 1150 °C to 1325 °C for the inverse exponential ramp. The average size and density of the voids as observed by SEM is reported in Fig. 3.

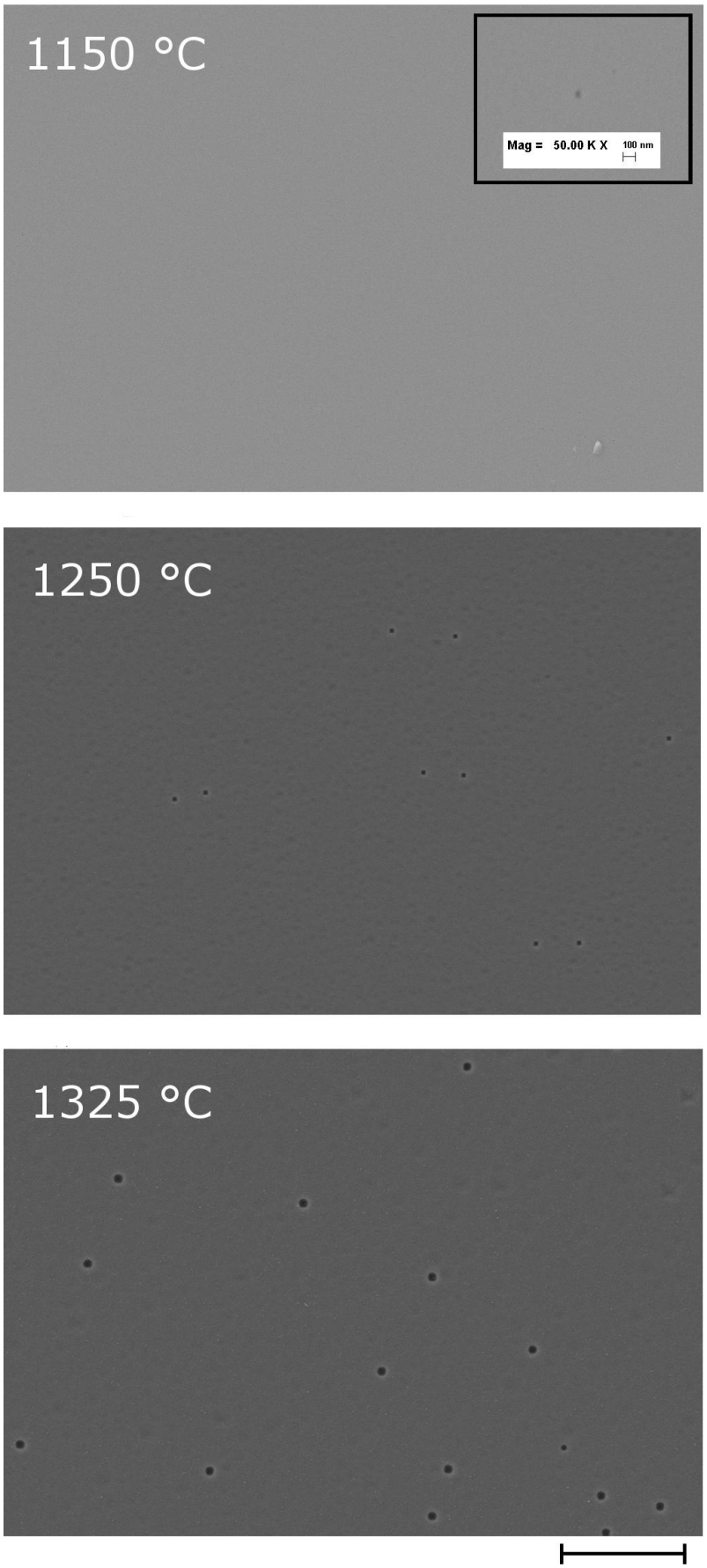
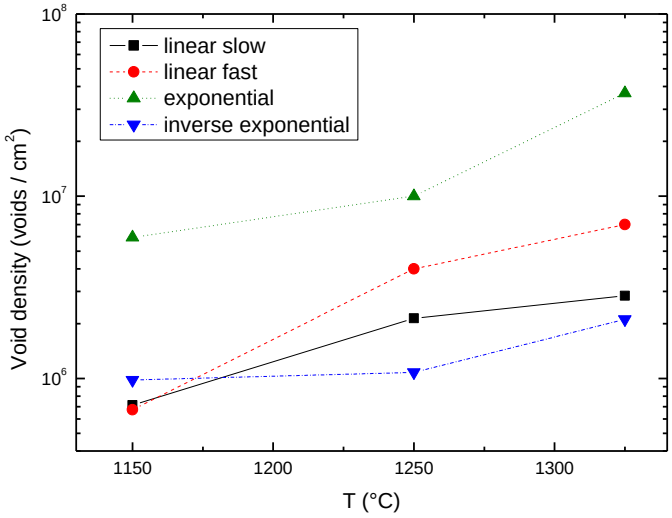
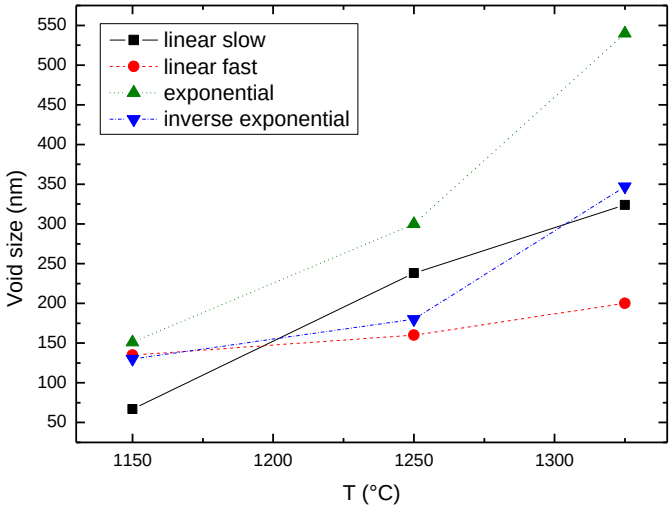


Fig. 2: Evolution of the voids using the linear slow ramp, stopping the process at different temperatures. The inset in the top images shows a void spotted with higher magnification. Marker is 5 micron



a)



b)

Fig. 3 a) average voids density and b) average voids size as measured by analyzing SEM images of carbonized sample stopped at different temperatures using different heating ramps. The lines are guide for the eye.

Fig. 4 shows how the different ramp shapes influence the void formation when the process is stopped at 1325 °C. At this stage the voids were big enough to be easily identified at the optical microscope. It seems evident that the exponential ramp gives the worst results in terms of voids density and the inverse exponential one provides the lowest density. At this temperature very few differences are seen between the two linear ramps (fast and slow), indicating that most of the voids are generated at higher temperatures.

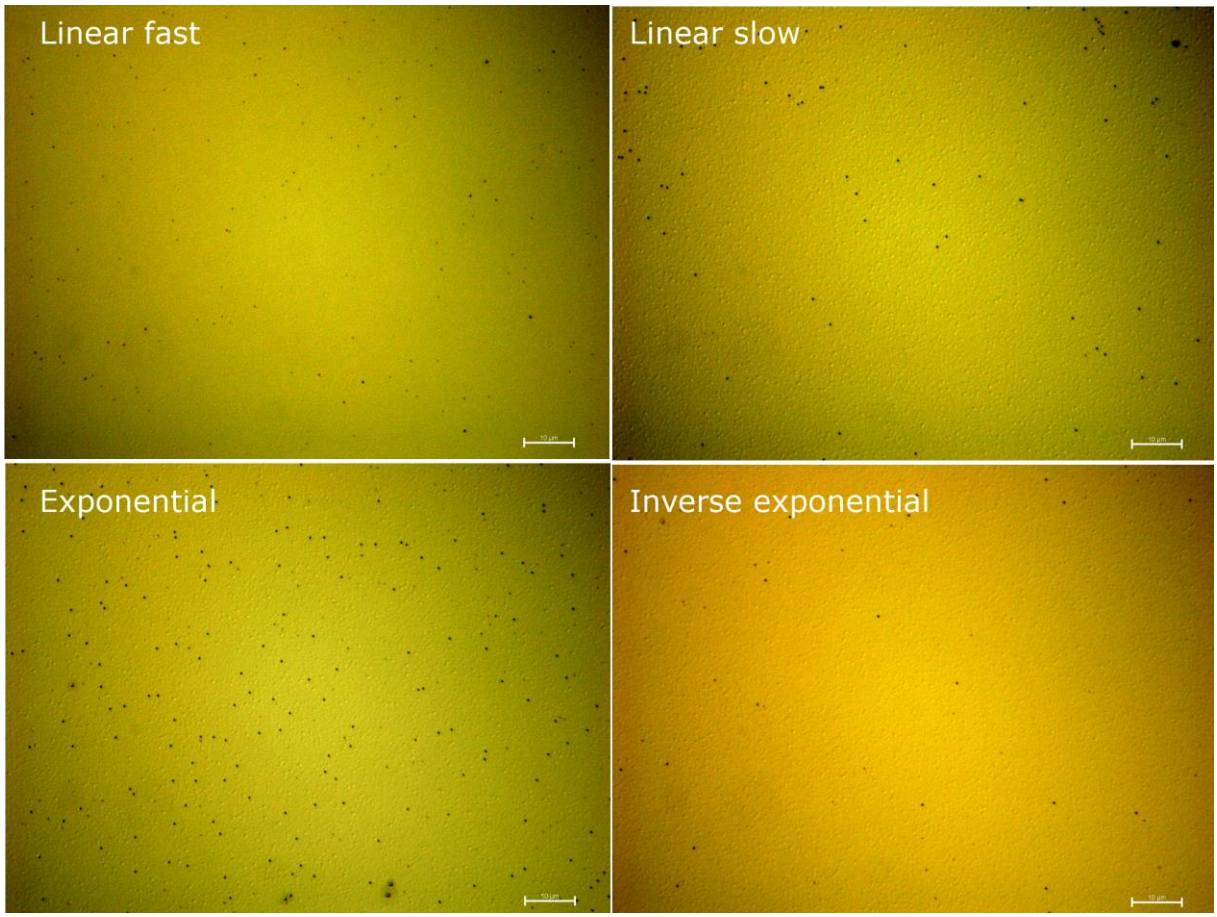


Fig. 4: optical microscope images of carbonization processes performed with different ramp shapes and stopped at 1325 °C. Voids appears here as dark spots. The marker is 10 microns for each images.

In order to compare the full carbonization processes, a standard SiC film on each of the four ramp types was deposited, in order to protect the carbonized surface and to avoid unwanted generation of voids due during the cooling down. Fig. 6 shows the SiC/Si interface of the different samples as observed in cross section by SEM: by investigating different areas of the samples it appeared that the linear slow ramp and the exponential ramps are generating about an order of magnitude less voids with respect to the other two ramps. A slower carbonization heating rate, expecially at higher temperature, is thus able to reduce voids formation.

It is generally recognized that voids at the SiC/Si interface are formed due to an etching process of silicon atoms from the substrate, promoted both by the temperature and by chemical reactions involving H_2. The gas phase is thus enriched with silicon atoms that, along with the C supplied by ethylene, contribute to the thin SiC layer formation [5,14,17,24]. From our experiments, that maintain constant the H_2 and C supply, it appears that the ramp shape and thermal effects have a main role in controlling the silicon out diffusion, the etching process and the formation of the SiC layer that seal the surface, preventing further silicon desorption, void formation and enlargement.

Si out diffusion from the substrate trought the SiC overlayer is a complex mechanism that strongly depends on process conditions and on the quality of the layer formed during the carbonization itself [25]. A good SiC carbonization layer, monocrystalline, compact and with a full coalescence and sealing of the Si substrate decreases the probability and paths for Si atoms to out diffuse, thus reducing the density and size of voids. Neverthelss, an incomplete SiC conversion of the Si substrate during the initial carbonization plateau or during the heating up towards the final growth temperature may leave open channels throught which Si out diffusion may be favoured [26]. For this reasons, literature usually reports that the best carbonization layers obtained using propane only are only several nm thick [5].

As expected, we observed that after the carbonization process the voids are always in the Si substrate and are generally covered by a very thin SiC layer: Fig. 7 is a typical SEM image of a sample grown

with the fast ramp, in which the carbonization layer extends also over the voids. We can also speculate that, due to the large difference in thermal expansion coefficient between SiC and Si (the SiC one being higher), the fast heating rate affects the mechanical stability of the carbonization layer more than a slower heating rate. We hypothesize that the faster ramp, expecially at higher temperatures, may induce very small cracks in the SiC layer, resulting in a partially open / not completely coalesced SiC carbonization layer that leaves paths for silicon to out diffuse from the substrate towards the gas phase.
In order to understand how the ramp shape influences the void generation it is convenient to model the carbonization process into two different stages: nucleation of a SiC seed layer at low temperature followed by enlargment and growth of these initial seeds at higher temperature, to form a continuous layer. [10,14,27] It is not straightforward to identify a definite temperature boundary between these two regimes but several papers report it around 1200-1250 °C, the temperature at which voids with appreciable size can be observed at SEM and optical microscope.
The ramp time used to move from low to high temperature has a huge effect in controlling the transition from the nucleation to the growth regime: Fig. 5 indicates the different mechanisms that may be involved in voids formation and suppression associated with the different thermal ramps adopted for the carbonization.
If we consider also the void density and size reported in Fig. 3a and Fig. 3b, we can suppose that for all the ramps, except the exponential one, the nucleation step is very similar: the void density measuread at 1150 °C is practically the same, about 10^6 cm^{-2} for three of the used ramps. The exponential ramp keeps the layer at low temperature for a longer time, thus we can argue that a longer nucleation step at low temperature is very inefficient in sealing the surface, probably because the silicon etching rate is higher than the nuclei enlargement rate. Also, a very poor coalescence of the nuclei is obtained, due to the very limited mobility of the adatoms on the substrate surface at low temperature.
With the fast linear ramp we can suppose that the transition between the nucleation and the growth regime occurs too fast, and the limited time available to reach the final growth temperature is not sufficient for the nuclei to enlarge and to completely coalesce to form the continuous layer needed to stop silicon out diffusion. Moreover, if we consider also the thermal mismatch, the fast ramp may also be non optimal to accommodate the lattice deformation of SiC with respect to Si, thus forming small cracks and openings in the already deposited carbonization layer. This may create more channels to permit to the Si atoms to diffuse from the substrate and explains also the increase in void density observed at 1325 °C in Fig. 3a. The same effect, given by thermal mismatch, can be observed by using the exponential ramp, because in the high temperature regime has slope similar to the linear fast one.
On the other hand, the linear slow and the inverse exponential ramps may provide both the optimal tranistion time between the nucleation and the growth regime and also the optimal time to accommodate the thermal mismatch, resulting in the lowest void density and similar void size.

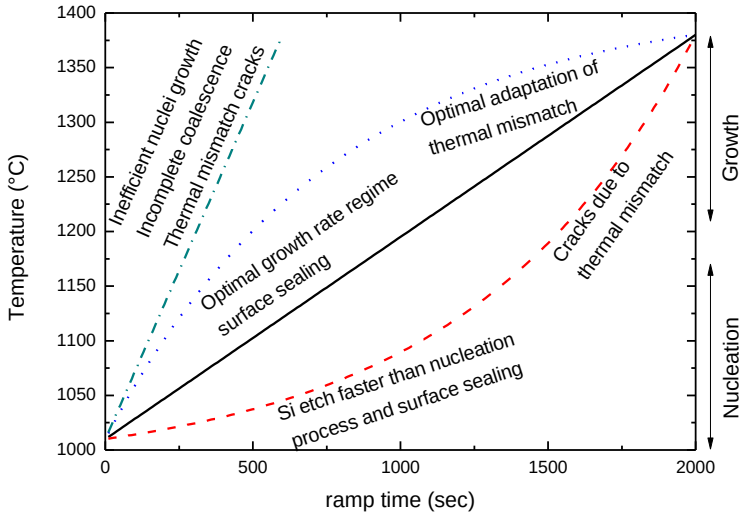


Fig. 5: Processes happening during the different heating ramps. See also Fig. 1 for reference.

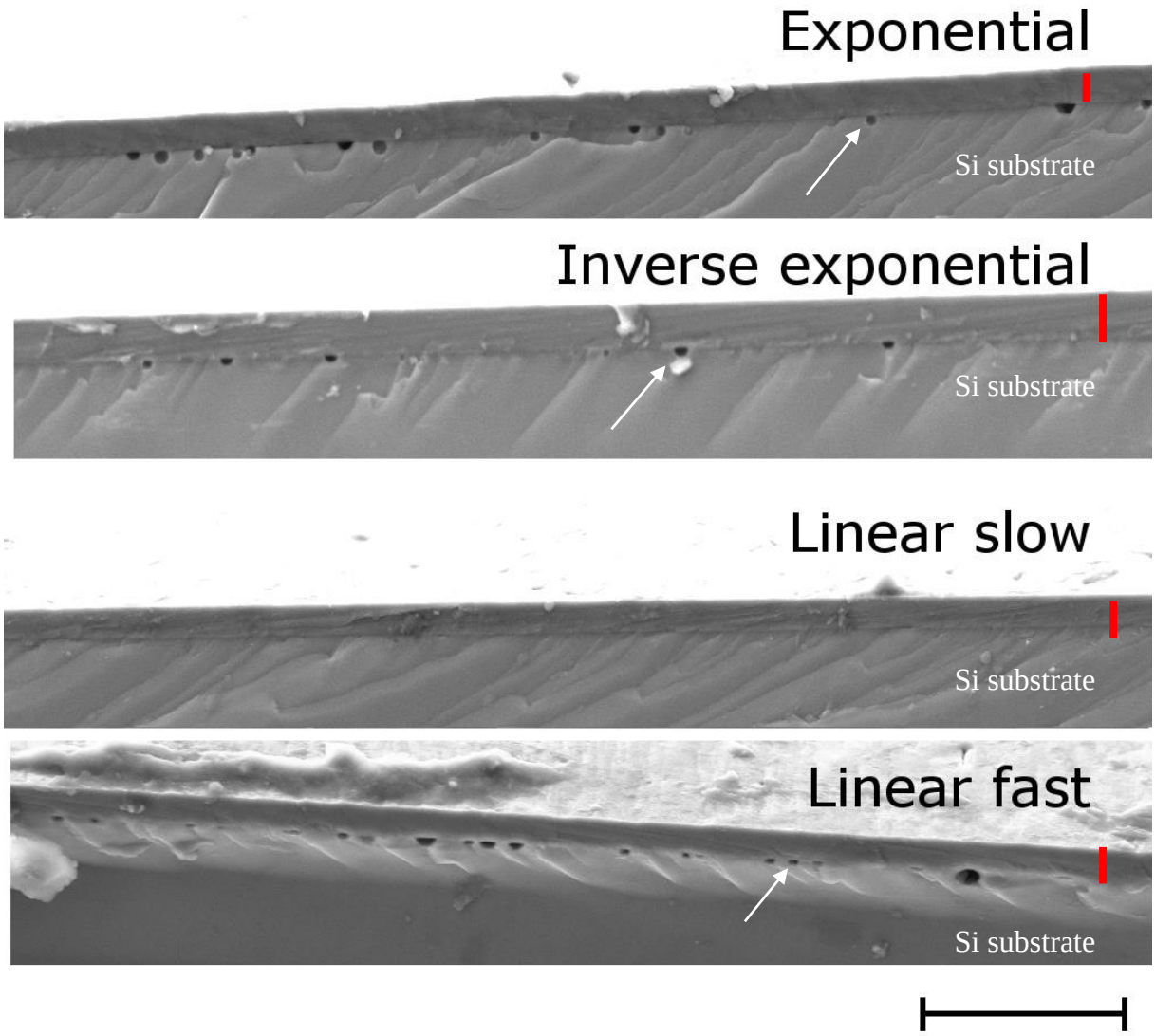


Fig. 6: SEM cross section of SiC films grown on different carbonization ramps. The arrows indicates a typical void, while the red bar indicates the SiC film. The marker is 5 microns.

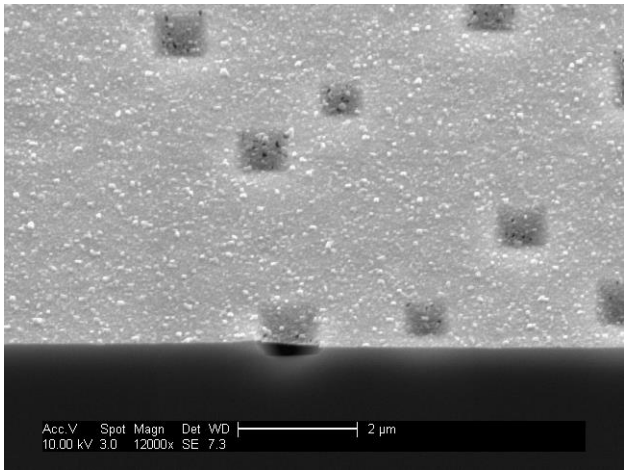
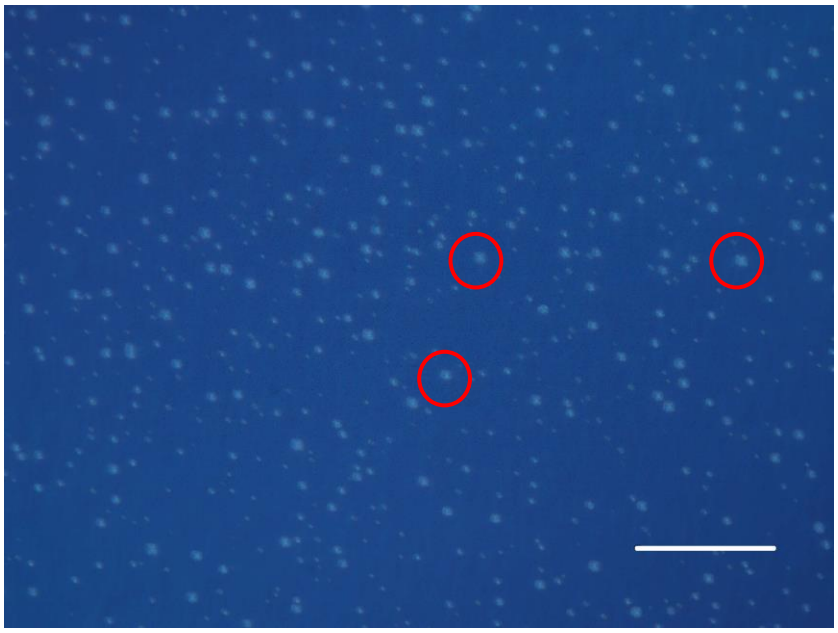


Fig. 7: Cross section SEM image of a carbonization layer obtained with the fast ramp. The SiC carbonization layer is evident in the area over the voids.

The simple idea of changing the ramp time was immediately implemented in the production reactor and an improvement on the void density was observed also in the different epitaxial system. Void density decreased by about an order of magnitude from about roughly 10^7 pits / cm^2 to 10^6 pits/cm^2, while maintaining the same SiC layer quality. Fig. 8 shows the differences between void density of two standard production SiC/Si wafer grown with different carbonization conditions, as observed by optical microscope.



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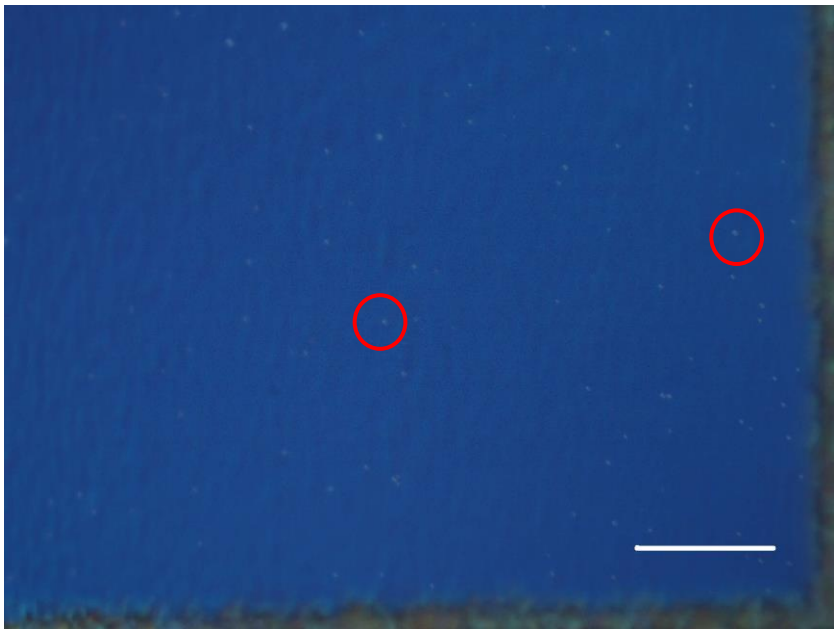

b)

Fig. 8: optical microscope image of a SiC film grown with a) the standard production process using a fast heating ramp from carbonization temperature to growth temperature, b) doubling the duration of the heating ramp. The red circles marks the interfacial voids, while the scale bar is 20 microns.

In order to reduce the Si out diffusion, the addition of a small flow of SiH_4 during the ramp up to growth temperature is a commonly used procedure, in order to introduce a slight Si overpressure in the gas phase that counterbalance the tendency of Si to desorb from the substrate [17,28]. The temperature at which SiH_4 is introduced, as well as its flow, are important parameters: if the SiH_4 flow is too high

and/or it is introduced at too low temperature, CVD growth of a low quality SiC may occur, thus degrading the final layer quality.
We initially tried to inject SiH_4 right after the carbonization plateau at 1000 °C and grow a standard SiC layer at 1380 °C, but the resulting film was found to be very hazy and polycrystalline. Moreover, the process resulted in a significant coating of poly material also in the graphite growth chamber. To avoid this problem we increased the temperature at which SiH_4 was injected and studied how adding this precursor in different moments of the ramp influences void formation.
Fig. 9 shows the comparison, as observed by SEM, of different SiC films grown over a linear slow carbonization ramp and with SiH_4 injected at different temperatures, from 1200 °C to 1325 °C. The sample with SiH_4 introduced at 1200 °C, althought with very few voids spotted at the interface, resulted in a surface with higher surface roughness, because the SiC optimal deposition temperature is not yet reached. With SiH_4 injected from 1250 °C the film quality was very similar but at 1300 and 1325 °C a slightly higher void density was observed. For this reason, the optimal SiH_4 injection temperature was chosen to be at 1250 °C. Considering the above discussion about nucleation and growth, the addition of SiH_4 to the gas phase should then occur near the temperature at which the growth regime starts.
The ramp shape has little influence on the generation of voids when SiH_4 is introduced at 1250 °C (Fig. 10), indicating that the generated Si overpressure during the carbonization is an effective means to suppress void formation and silane oudiffusion from the substrate. The presence of SiH_4 in the gas phase may also help in enlarging the seeds formed at lower temperature and helps in growing a higher quality SiC layer. The presence of a controlled source of Si in the gas phase may be also helpful to stabilize the grow process.
The fact that voids can be almost completely eliminated also using a fast carbonization ramp (10 minutes) instead of a longer one (30 minutes) is also a particularly important results because it would mean to reduce the time and the cost of the production process.

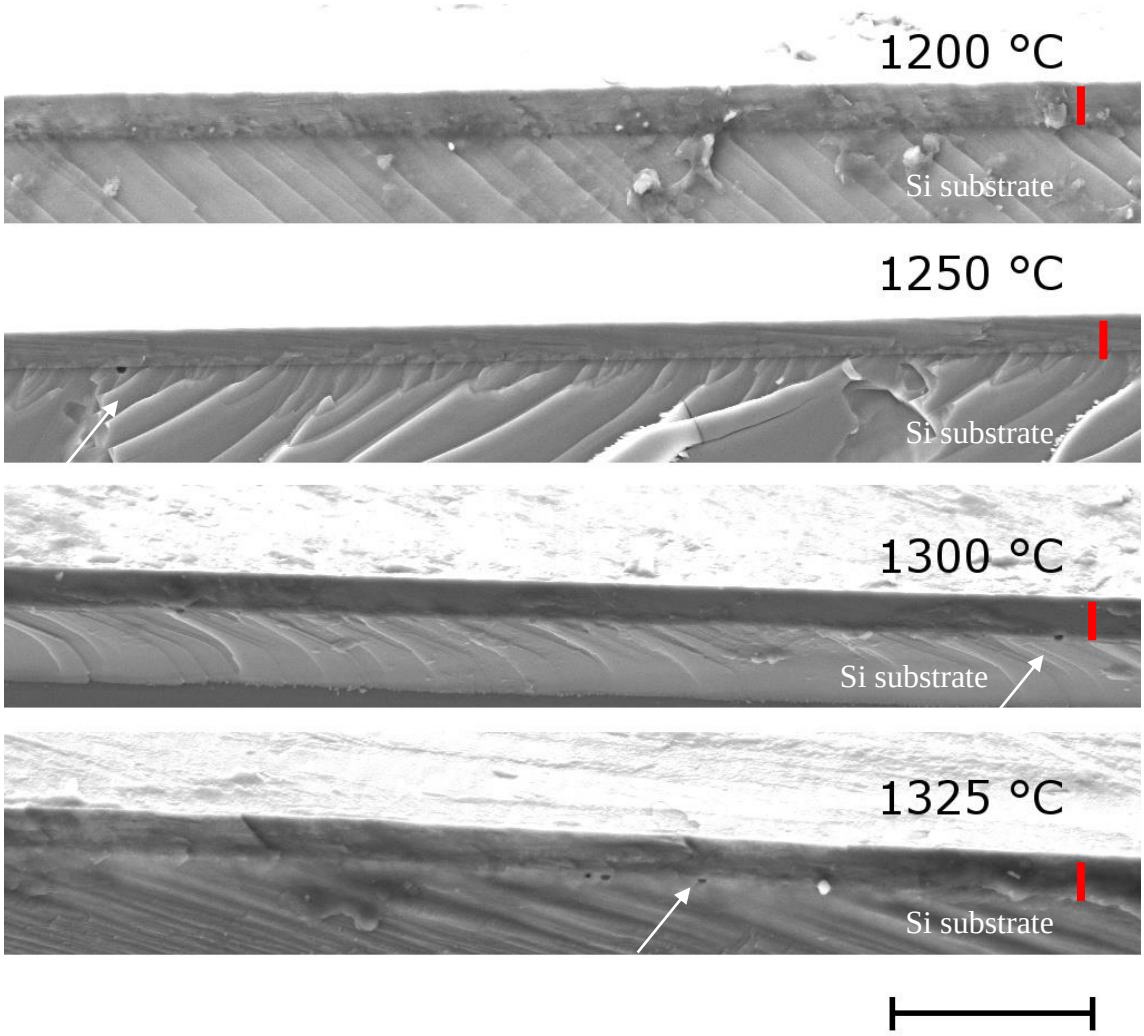

Fig. 9: SEM cross section of SiC films grown with SiH_4 injected at different temperatures, using the linear slow ramp. The red lines indicate the SiC film while the marker is 5 microns.

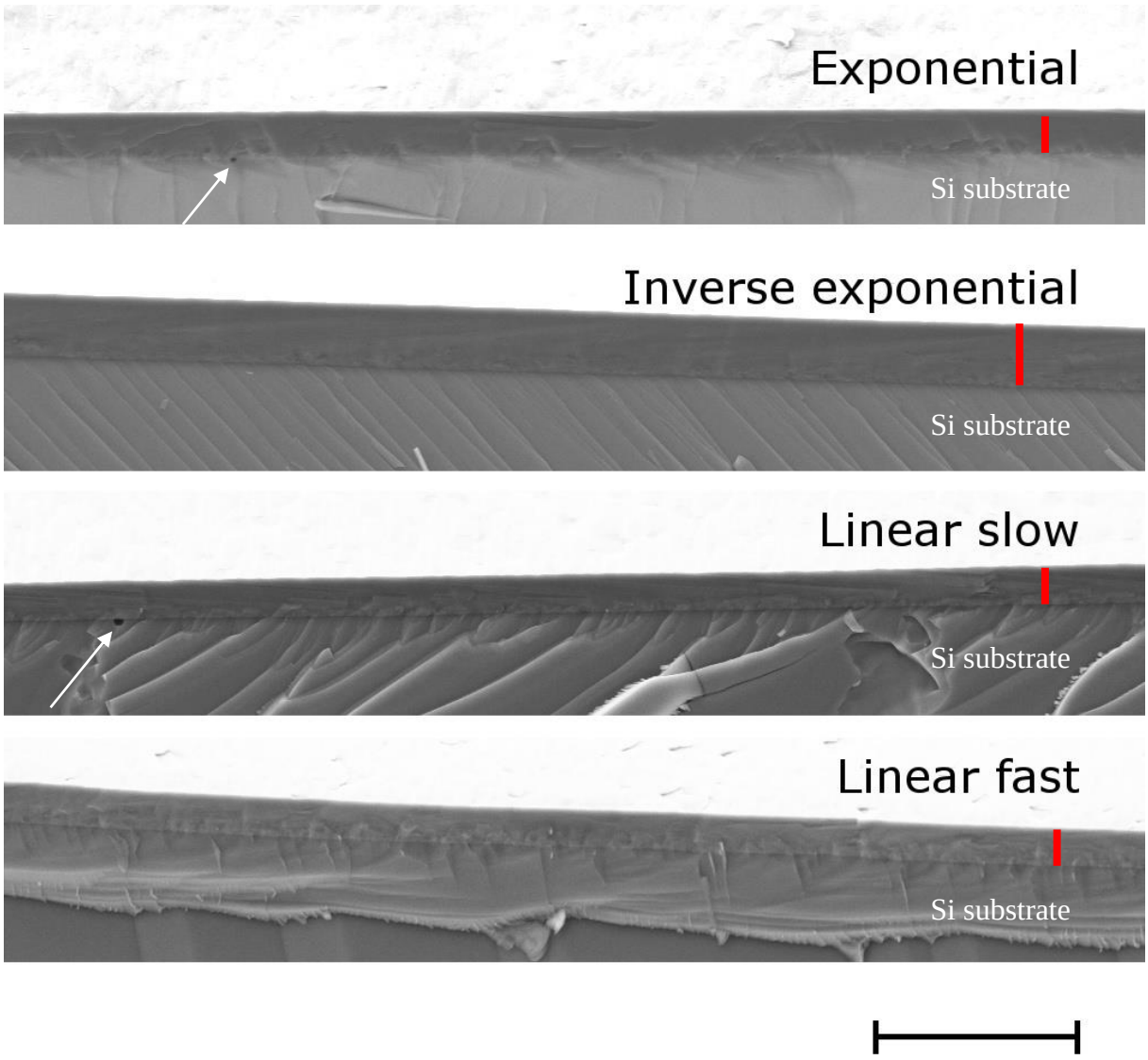

Fig. 10: SEM cross section of SiC films grown with SiH_4 injected 1250 °C, using different ramp shapes. The red lines indicate the SiC film while the marker is 5 microns.

Finally, we studied the effect of different SiH_4 flows rate during the fast carbonization ramp, starting to inject the gas at 1250 °C (Fig. 11): It appears that the lower SiH_4 flow regimes are not able to effectively suppress void formation, mainly because the Si partial pressure in the gas phase is not high enough to prevent Si etching from the substrate.

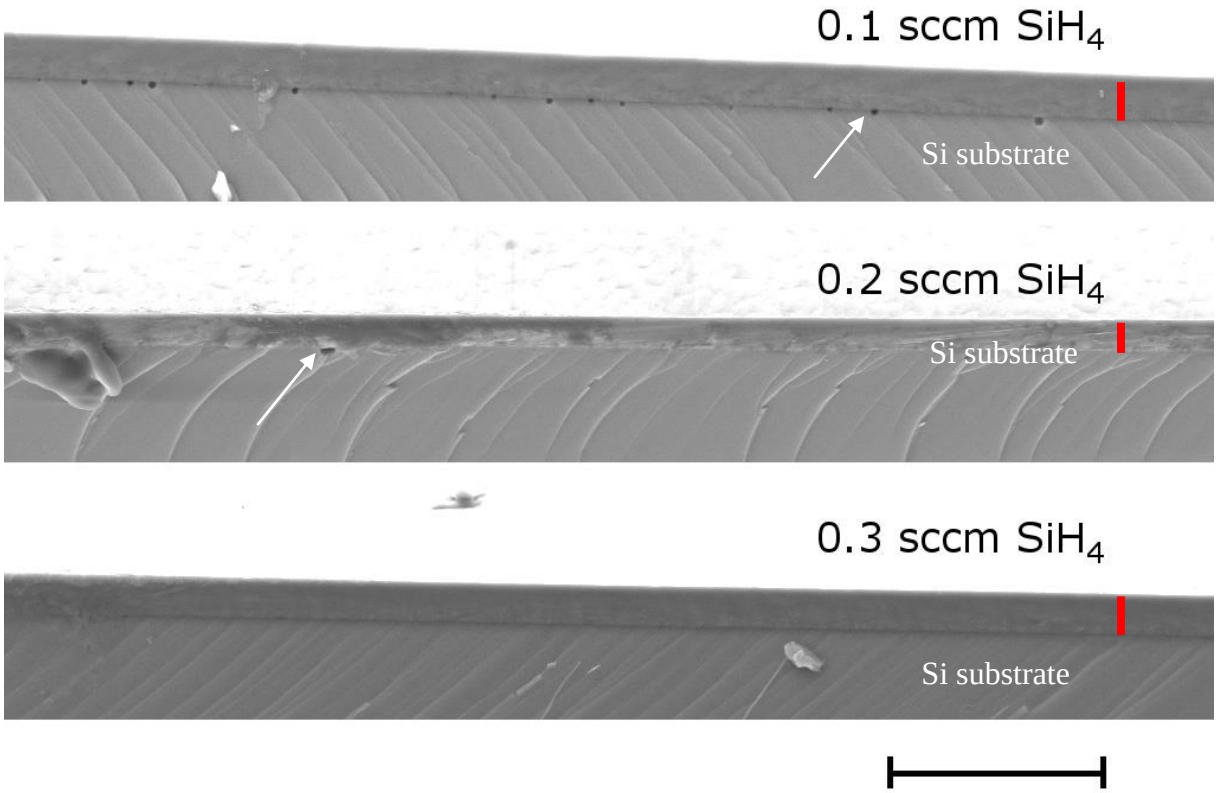

Fig. 11: SEM cross section of SiC films grown with different SiH_4 flows, injected at 1250 °C, using the fast linear ramp. The red lines indicate the SiC film while the marker is 5 microns.

Once the optimal conditions for the injection of SiH_4 during the heating ramp were identified (injection temperature and flow regime), they were reproduced in the production reactor and compared with the standard process, before optimization. A SiC/Si film, about 8.5 μm thick, was grown on a 100 mm substrate and the observation at the optical microscope of the SiC/Si interface (Fig. 12) showed an impressive reduction of voids density if compared with the standard process (Fig. 8). XRD measurements (Fig. 13) were performed in order to compare the lattice quality of the two layers: the full width at half maximum of the two samples is respectively of about 340 and 357 arcsec, indicating a overall similar lattice quality.

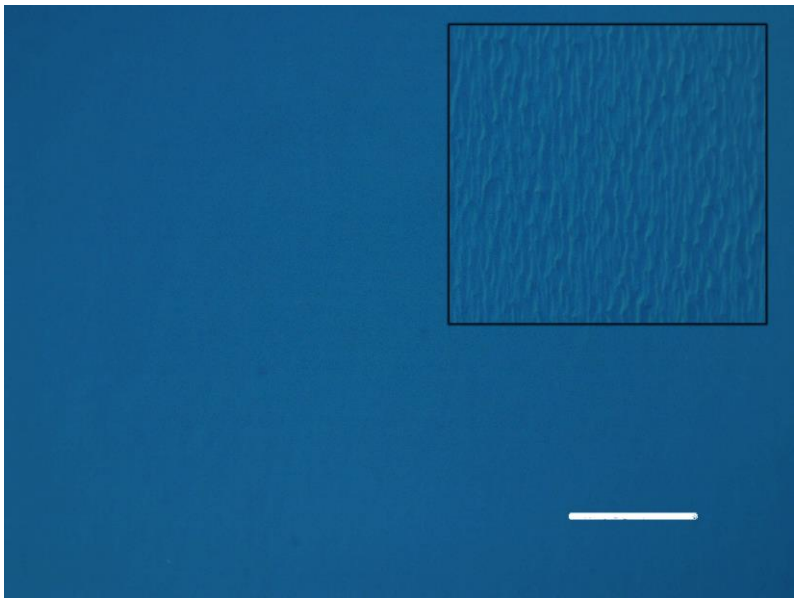

Fig. 12: optical microscope image of a SiC/Si film (about 8,5μm thick) grown in the production reactor by introducing a SiH_4 flow at during the heat up from carbonization to growth temperature. The main image is focussed on the SiC/Si interface while the inset is focussed on the surface. The scale bar is 20 microns for both images.

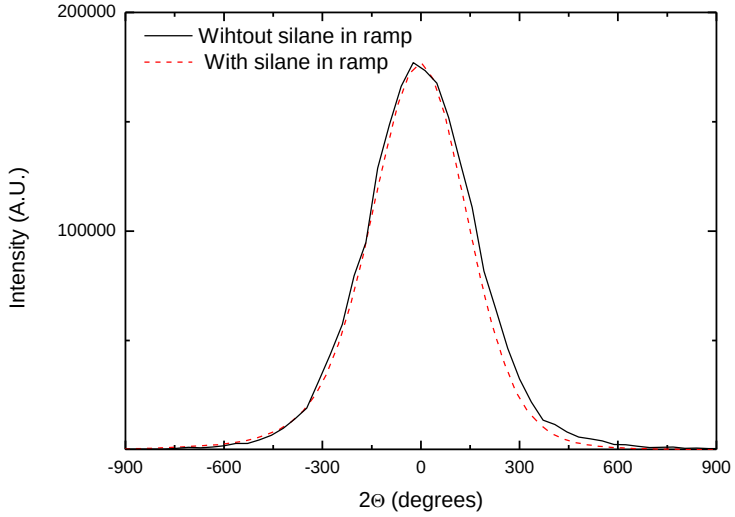

Fig. 13 Comparison of the XRD diffractograms (normalized for clarity) of 100mm epi-wafers deposited in the production reactor, grown with and without SiH4 during the temperature ramp. The FWHM of the two layers are 340 and 357 arcsec, respectively.

Conclusions

A comprehensive study of the carbonization process for the deposition of SiC epilayer on on Si (001) 4° misoriented substrates was presented. In order to reduce production development cost and time, the experiments were initially performed on a small research VPE reactor, exploring a large range of parameters involving different thermal ramp rates and shapes to heat the substrate from carbonization temperature (1000 °C) to growth temperature (1380 °C). The process was stopped at different stages to study how voids form and evolve with the temperature. It was noted that a too fast heating ramp (10 min) generated a lot of voids while a linear slow ramp (30 min) resulted in about an order of

magnitude less voids. It was found important to reduce the heating rate of the substrate when it reaches temperatures higher that 1250-1300 °C, and an inverse exponential heating ramp was adopted to minimize voids formation.
Furthermore, voids were almost completely eliminated by the introduction of silane at 1250 °C during the heating ramp, regardless of the ramp shape used to heat the substrate. This process permitted to deposit thick SiC/Si layer with similar lattice quality of the one without the use of silane but with negligible void density.
After having understood the variables involved in the process using the research reactor, the key ideas were successfully transferred to a 100 mm production reactor and SiC layers with very small void density was obtained.

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