Interface electrical properties of Al_2O_3 thin films on graphene obtained by atomic layer deposition with in–situ seed-like layer

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Abstract

High quality thin insulating films on graphene (Gr) are essential for field effect transistors (FETs) and other electronics applications of this material. Atomic Layer Deposition (ALD) is the method of choice to deposit high-κ dielectrics with excellent thickness uniformity and conformal coverage. However, to start the growth on the sp^2 Gr surface a chemical pre-functionalization or the physical deposition of a seed layer are required, which can effect, to some extent, the electrical properties of Gr. In this paper we report a detailed morphological, structural and electrical investigation of Al_2O_3 thin films grown by a two-steps ALD process on a large area Gr membrane residing on an Al_2O_3/Si substrate. This process consists of the H_2O-activated deposition of few nanometer Al_2O_3 seed layer performed in-situ at 100 °C, followed by ALD thermal growth of Al_2O_3 at 250°C. The optimization of the low-temperature seed layer allowed to obtain a uniform, conformal and pinhole free Al_2O_3 film on Gr by the second ALD step. Nanoscale resolution mapping of the current through the dielectric by conductive atomic force microscopy (CAFM) demonstrated an excellent laterally uniformity of the film. Raman spectroscopy measurements indicated that the ALD process does not introduce defects in Gr, whereas it produces a partial compensation of Gr unintentional p-type doping, as confirmed by a threefold increase of Gr sheet resistance (from ~300 Ω/sq in pristine Gr to ~1100 Ω/sq after Al_2O_3 deposition). Analysis of the transfer characteristics of Gr field effect transistors (GFETs) allowed to evaluate the relative dielectric permittivity (ε=7.45) and the breakdown electric field (E_{BD}=7.4 MV/cm) of the Al_2O_3 film, as well as the transconductance and the holes field effect mobility (~1200 $cm^2V^{-1}s^{-1}$). A special focus has been given to the electrical characterization of the Al_2O_3/Gr interface by the analysis of high frequency capacitance-voltage measurements, which allowed to elucidate the charge trapping/detrapping phenomena due to near-interface and interface oxide traps.

Introduction

Due to its excellent electronic, optical, thermal and mechanical properties, graphene (Gr) holds great promises for future applications in the fields of electronics, optoelectronics and sensing. As a matter of fact, the integration of dielectric materials on top of graphene (Gr) represents a key requirement for many of these device applications. The thin insulating film can work as gate dielectric for top gated Gr Field Effect Transistors (GFETs) [1] or can act as tunnelling or thermionic emission barrier for recently proposed vertical devices, such as the Gr-Base Hot Electron Transistor (GBHET) for ultra-high frequency electronics. [2,3] In addition, insulating layers deposited on Gr can be profitably exploited for several other purposes, e.g., as an encapsulation to isolate Gr from external environment [4] or as an overlayer that can be properly functionalized to achieve specific chemical or biological selectivity for Gr-based sensors. [5] A tight control of the structural quality (thickness homogeneity and conformal coverage) and of the electrical performances (dielectric constant, leakage current, breakdown field,..) is mandatory in the case of transistors applications and can represent a key advantage for other applications.

Atomic layer deposition (ALD) is the method of choice to deposit dielectric films with extremely high control (atom by atom) on the thickness. However, the chemical inertness of the pristine (i.e., defect-free) Gr surface does not allow the chemisorption of the metalorganic precursors, which is necessary as the first step to initiate an ALD process. [6] Hence, to address this issue, the activation of Gr surface is typically required before the ALD growth. This kind of process can consist either in the physical deposition of a seed layer on Gr or in the direct modification of Gr surface. Furthermore, it can be performed ex-situ, i.e., externally from the ALD reactor chamber, or in-situ, i.e., inside the chamber. To date, several seed layers for ALD on Gr have been explored, including the deposition of a thin metal film, which is subsequently oxidized in air or by controlled exposure to oxygen, [7,8] or the direct deposition of few nanometres of a metal-oxide, [9] the coating by organic films, molecules or macromolecules [10] with proper affinity both with Gr and with the metalorganic ALD precursor. A second layer of Gr functionalized by O_2 plasma exposure and transferred onto Gr surface has been also employed as a seed layer for ALD. [11] The physical deposition of a seed layer commonly creates only a very limited amount of defects in the Gr membrane. However, since it is typically performed ex-situ, it can introduce impurities/particles that can be detrimental for the reliability of the dielectric film subsequently deposited by ALD. Furthermore, the use of a seed layer ultimately limits the possibility of scaling the thickness of the deposited oxide. An alternative seed-layer-free approach is based on the in-situ activation of Gr by physical adsorption of specific gas species, such as O_3 [12] or N_2O, [13] working as adhesion catalysers between Gr and the metalorganic precursor. However, in-situ functionalization of Gr with such reactive gas species needs to be properly tailored [14] to avoid the occurrence of chemisorption processes, leading to the introduction of defects in Gr and, consequently, to the degradation of its electronics properties.

Recently, an alternative method based on the in-situ deposition of a metal-oxide (HfO_2, Al_2O_3) seed layer assisted by H_2O has been proposed. [15,16] In this approach, the initial stage is the physical adsorption (by Van der Waals forces) on Gr of a continuous layer of H_2O molecules, which work as activation sites for the seed layer deposition. In order to guarantee a uniform distribution of H_2O molecules over the Gr surface, it is necessary to operate within an adequate temperature window, i.e., not too low in order to avoid intermolecular attraction with a consequent water droplets condensation and the formation of local nucleation sites, not too high in order to prevent the escape of molecules due to excessive thermal excitation. Recent papers reported an optimal temperature window from 100 to 130°C for the growth of the Al_2O_3 seed layer using TMA/H_2O on Gr transferred on a SiO_2 substrate. [16] It is worth noting that this temperature range is far below the optimal range for thermal ALD of Al_2O_3, resulting in a poor structural/electrical quality of the seed layer. For this reason, after the low temperature in-situ deposition of the seed layer, the ALD growth of the Al_2O_3 film was completed

by a second step carried out at higher temperatures (200 – 250 °C), resulting in an uniform dielectric film with good dielectric performances (relative dielectric permittivity ε=7.2, breakdown electric field up to 9 MV/cm). [17] The uniformity of the Al_2O_3 thin films obtained by this two-steps in-situ deposition was demonstrated to depend crucially on the initial morphology of the seed layer. [17] It was also observed that the H_2O – assisted ALD of Al_2O_3 gives rise to a reduction of the unintentional p-type doping of Gr transferred onto SiO_2, or even to n-type doping. [18]

In view of these promising aspects of two-steps in-situ ALD processes, a complete electrical characterization of top-gated GFETs with Al_2O_3 dielectrics deposited by this approach would be highly desirable. In particular, a study of the interface or near-interface traps present in the interfacial region between Gr and Al_2O_3 and of the charge trapping/detrapping phenomena responsible of hysteresis during transistor operation is still missing. Clearly, such investigation is mandatory to get a better understanding of the electrical properties of the dielectric material for transistor applications.

In this paper we report a detailed morphological, structural and electrical characterization of Al_2O_3 thin films grown by an optimized two-steps ALD process (consisting of H_2O-assisted seed later deposition at 100 °C, followed by ALD deposition at 250 °C) on large area Gr membranes on an Al_2O_3/Si substrate. The optimization of the low-temperature seed layer deposition step allowed us to obtain a uniform (i.e., low roughness, pinhole-free) and conformal Al_2O_3 film on Gr by the second ALD step, as demonstrated by atomic force microscopy (AFM). In addition, nanoscale resolution mapping of the current through the dielectric film by conductive AFM showed an excellent electrical uniformity with negligible leakage current for the typical electric fields applied to the gate dielectric during transistor's operation. Raman spectroscopy measurements indicated that the ALD process does not introduce defects in Gr, whereas it produces a partial compensation of unintentional p-type doping. This was confirmed by the increase of Gr sheet resistance (from ~300 to ~1100 Ω/sq) after the ALD deposition, evaluated by transmission line model (TLM) test structures. Current-voltage characterization of GFETs allowed to evaluate the relative dielectric permittivity (ε=7.45) and the breakdown electric field (E_{BD}=7.4 MV/cm) of the Al_2O_3 film on Gr, as well as the transconductance and the holes field effect mobility (~1200 $cm^2V^{-1}s^{-1}$). Finally, high frequency capacitance-voltage measurements on the transistors were used to investigate the charge trapping mechanisms due to near-interface and interface states of the dielectric, and to evaluate the interface trapped charge density.

Experimental details

Single layer Gr samples grown on copper foils by chemical vapour deposition (CVD) were used in our experiments. Gr membranes were transferred to the target substrate (a Si wafer coated by ~97 nm of Al_2O_3 deposited by sputtering) using the standard transferring procedure, i.e., PMMA coating, chemical etching of copper and Gr fishing. Careful cleaning of the Gr surface was carried out after transfer by a sequence of baths in acetone and isopropanol in order to remove polymer residues. The two steps ALD of Al_2O_3 on Gr was carried out using a Plasma Enhanced-ALD LL reactor by SENTECH Instruments GmbH. First, a careful optimization of the seed layer deposition parameters at low temperature (100°C) was carried out, focusing on the role of the precursor exposure time and purging time. After setting the optimal conditions for a uniform seed layer, the second ALD step at higher temperature was carried out at 250°C. The same deposition processes performed on Gr were also carried out on lowly doped Si samples (10^{15} cm^{-3}), which were used as reference for structural and electrical characterization. Tapping mode atomic force microscopy (tAFM) measurements, using a DI3100 system and Si tips, were employed to monitor the surface morphology and evaluate the roughness of the samples. Raman spectroscopy with a laser source at 532 nm wavelength was used to monitor both the defects density and doping effects on Gr after each deposition step, i.e., after the seed layer deposition at low temperature and the complete

Al_2O_3 film growth. Nanoscale resolution current mapping and local current-voltage characterization of the seed layer and of the final Al_2O_3 films deposited on Gr were carried out by Conductive Atomic Force Microscopy (CAFM) using metal (Pt) coated Si tips. Furthermore, properly designed device structures were employed to evaluate the Gr electrical properties on a macroscopic scale. In particular, transmission line model (TLM) devices, consisting of Gr rectangular stripes with Ni/Au contacts at different distances, were measured before and after the Al_2O_3 film deposition, in order to evaluate changes in the Gr sheet resistance due to the ALD process. Finally, Gr field effect transistors (GFETs) with channel widths W_{ch} from 100 to 150 μm and channel lengths L_{ch} from 15 to 45 μm have been fabricated. DC current-voltage measurements on the GFETs have been performed to evaluate the Gr field effect mobility and the electrical properties of the Al_2O_3 top gate dielectric on Gr (permittivity, breakdown field). High frequency (1 MHz) capacitance-voltage (C-V) analyses were carried out to evaluate the density of interface trapped charges responsible of the hysteresis of GFETs electrical characteristics.

Results and discussion

1. Deposition process

The H_2O-assisted deposition of the Al_2O_3 seed layer within the ALD chamber was carried out by performing an initial number of H_2O cycles, up to the formation of a uniform wetting layer of physically adsorbed H_2O molecules on Gr, followed by cycles with TMA and H_2O at low temperature for the deposition of Al_2O_3. In our process, the optimal conditions for the formation of this seed layer have been established using a fixed number of H_2O pre-treatment cycles and H_2O/TMA low temperature cycles, and progressively increasing the precursors exposure and purging periods. The coverage and homogeneity of the Al_2O_3 seed layer was evaluated by ex-situ tAFM morphological measurements. Fig. 1(a) reports the starting morphology of Gr transferred on the Al_2O_3/Si substrate. Fig. 1(b-d) report the tAFM morphologies of the Al_2O_3 seed layer deposited on Gr by 6 H_2O pre-treatment cycles, followed by 60 H_2O/TMA cycles at 100°C, considering incrementally long exposures and purging periods for both reagents (TMA and H_2O) as described on the horizontal axis above the Fig. 1(b-d). A seed layer with optimal coverage and homogeneity has been obtained for precursors exposures of 100 ms and purging periods of 6000 ms. For these deposition conditions, the low temperature seed layer reveals a roughness of 0.53 nm, comparable to the starting bare Gr roughness (0.37 nm).

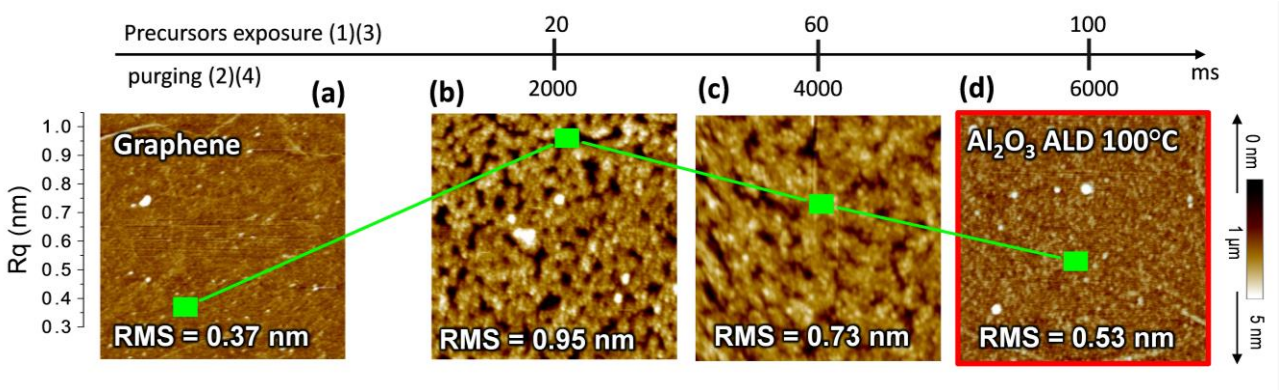

Figure 1: (a) tAFM of Gr transferred on the Al_2O_3/Si substrate, (b-d) tAFMs of the Al_2O_3 seed layer deposited by 60 cycles of an ALD process at 100°C, considering incrementally long precursors exposures and purging periods. The horizontal axis reports (1) the TMA exposure period, (2) the TMA excess purging period, (3) the H_2O exposure period, (4) the H_2O excess purging period. The vertical axis reports the root mean square (RMS) roughness estimated by the AFM images.

After setting the optimal seed layer deposition conditions, a second Al_2O_3 layer was deposited at higher temperature of 250 °C by performing 250 TMA/H_2O deposition cycles. The full thickness of the stack was ~22 nm, as deduced by cross-sectional TEM analyses and ellipsometric measurements on films deposited under the same conditions on a reference Si substrate (as discussed later on in this section). In order to evaluate the coverage conformity of the obtained film on single layer Gr, the two-steps deposition was carried out on a Gr membrane transferred on the Al_2O_3/Si wafer and patterned by photolithography and O_2 plasma etching. Fig. 2(a) and (b) report a schematic illustration and the tAFM image of the patterned Gr, respectively. The measured step height obtained after an O_2 plasma etch at 300 W for 30 s is 2.16 nm. As a matter of fact, the etching process not only removes Gr but causes also a small overetch (1.6 - 1.7 nm) of the underlying Al_2O_3 substrate. Hence, the measured step height is the sum of the monolayer Gr thickness and of the Al_2O_3 overetch. Fig. 2(c) reports a high resolution tAFM image of Gr and a surface roughness of 0.37 nm. This roughness values is partially due to the Al_2O_3 substrate roughness (~0.28 nm) and partially to the presence of wrinkles, typical corrugations of transferred CVD Gr. A larger area (20 μm×20 μm) AFM image of Gr on Al_2O_3/Si is reported in Fig. S1 of the Supporting Information. The density and the typical height (1-3 nm) of Gr wrinkles, as well as the presence of small PMMA residues from the transfer, can be evaluated from this image. Fig. 2(d) and (e) report a schematic illustration and the tAFM image of the patterned Gr after the Al_2O_3 growth by the two-steps ALD process. The step height is ~1.2 nm, just slightly lower than the previous data, confirming that the growth of the dielectric regularly occurs on Gr. The reduced step height suggests a certain delay of the first cycles of ALD growth on Gr with respect to the bare Al_2O_3 surface. It is worth noting that the typical morphology of the CVD-Gr, that is characterized by the presence of few nanometres height wrinkles, is still visible in Fig. 2(e) after the deposition of ~22 nm of Al_2O_3, confirming the very good conformal coverage of Gr surface. A higher resolution tAFM image is reported in Fig. 2(f), showing a continuous Al_2O_3 coating of Gr with a roughness of 0.55 nm, comparable with that obtained on bare Gr. Once more we want to stress that such a uniform Al_2O_3 coating is a consequence of the optimized low-temperatures in-situ seed layer. In fact, a very inhomogeneous coverage, with a high RMS roughness of ~6.7 nm, is obtained performing a total of 310 TMA/H_2O cycles directly at 250 °C, as shown in Fig. S2 of the Supporting Information.

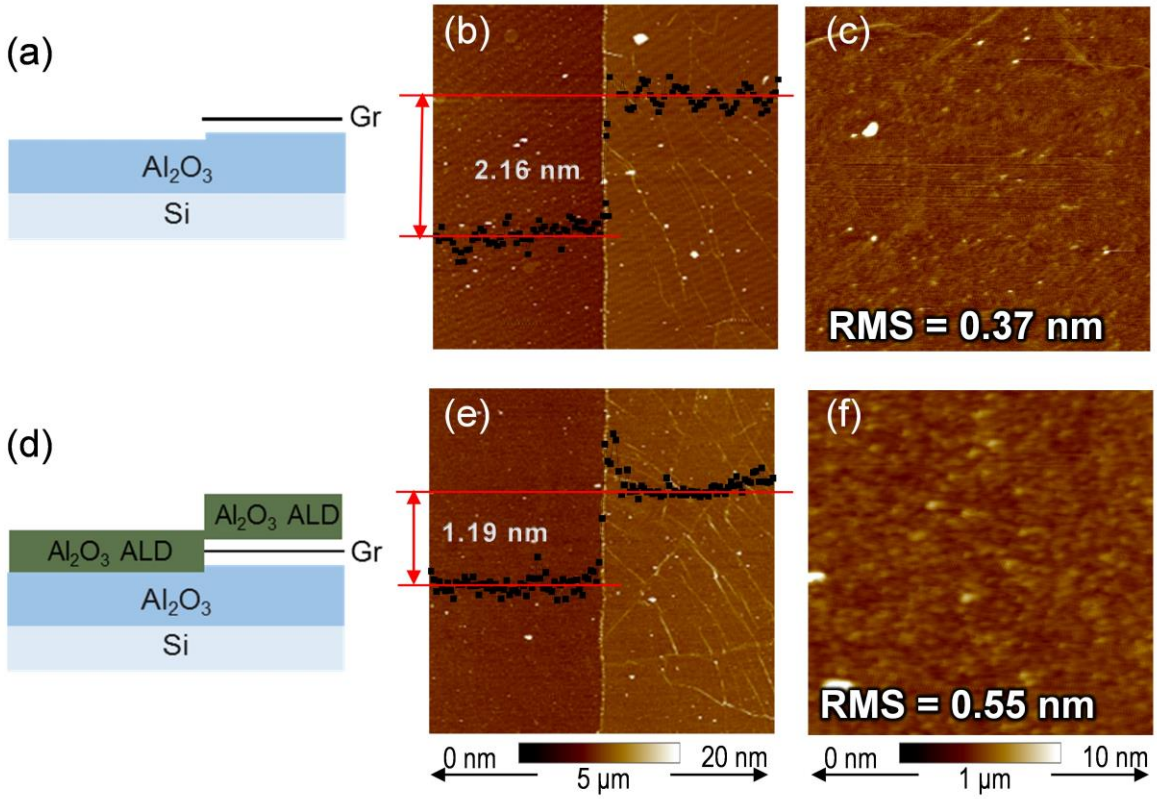

Figure 2: (a) Schematic illustration and (b) tAFM image of the patterned Gr on Al_2O_3 substrate. (c) High resolution tAFM image of Gr. (d) Schematic illustration and (e) tAFM image of the Al_2O_3 coated patterned Gr. (f) High resolution tAFM image of Al_2O_3 coated Gr.

The same deposition process was performed also on a Si reference sample. Fig. 3(a) reports the tAFM morphology of the bare Si substrate, with a roughness of ~0.2 nm measured on 1 µm^2 area. Fig. 3(b) shows the morphology after the low temperature deposition of the Al_2O_3 seed layer, showing an almost unchanged surface roughness (~0.2 nm). The seed layer thickness and the growth per cycle were characterized by ellipsometry at several positions on a 6 inches wafer, estimating a 4.7 ± 0.1 nm thick deposited seed layer, with a growth rate of 0.08 nm/cycle. Fig. 3(c) shows the tAFM morphology of the whole Al_2O_3 film after the two-steps deposition, revealing again a roughness of ~0.2 nm measured on 1 µm^2 area. A total film thickness of 21.84 ± 0.05 nm and a growth rate of 0.07 nm/cycle were evaluated by ellipsometry measurements at several wafers positions, as well as by TEM analyses on cross-sectioned samples.

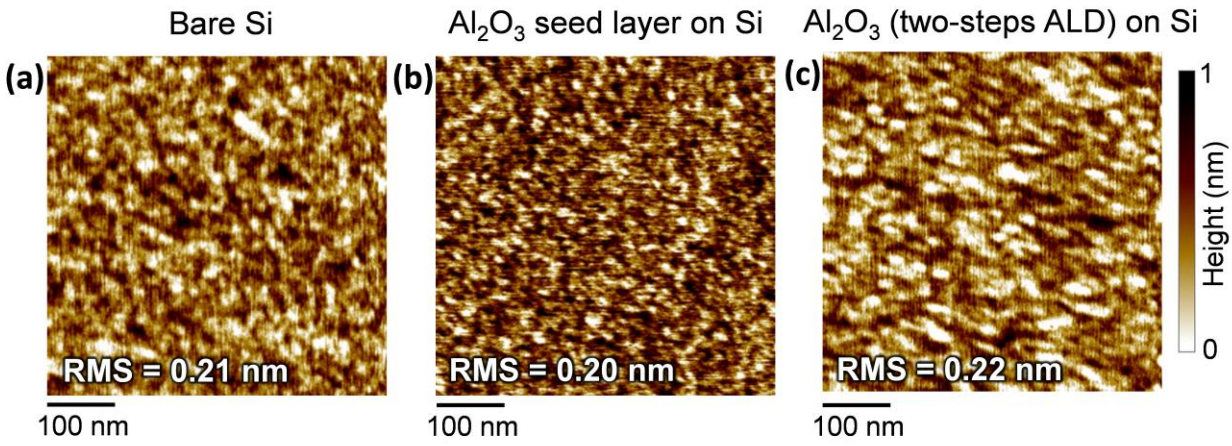

Figure 3: (a) tAFM morphology of the Silicon substrate, (b) tAFM morphology after the low-temperature Al_2O_3 seed layer deposition, (c) tAFM morphology after the two-steps Al_2O_3 deposition.

Raman spectroscopy analyses were performed to evaluate the effect of Al_2O_3 deposition on the Gr structural quality (defectiveness) and doping. Fig. 4 (a) shows three representative Raman spectra collected on bare Gr, after the Al_2O_3 seed layer deposition and after the complete two-steps deposition. Only a low intensity D peak (which is related to defects in Gr) can be observed in the as-transferred Gr and after each deposition step, thus indicating that the water-assisted seed layer deposition does not introduce significant damage in Gr. Furthermore, we observed an increase of the ratio between the 2D and G peaks intensities (I_{2D}/I_G) from 1.47 in the bare Gr sample to 1.52 after the seed layer deposition, and a further increase to 1.83 after the complete two-steps Al_2O_3 deposition (see Fig. 4(b)). This increase of the I_{2D}/I_G ratio is accompanied by a red-shift of the G peak position from 1595 cm^{-1} for bare Gr to 1593.5 cm^{-1} after seed layer deposition, and to 1592.5 cm^{-1} after the complete deposition (see Fig. 4(c)). This behaviour of the characteristic Raman peaks of Gr can be ascribed to a reduction of the starting unintentional p-type doping of transferred CVD-Gr, [19] consistently with the results of electrical characterization reported in the next section. Such an effect has been also reported by other authors after the deposition of the Al_2O_3 film on Gr. [20]

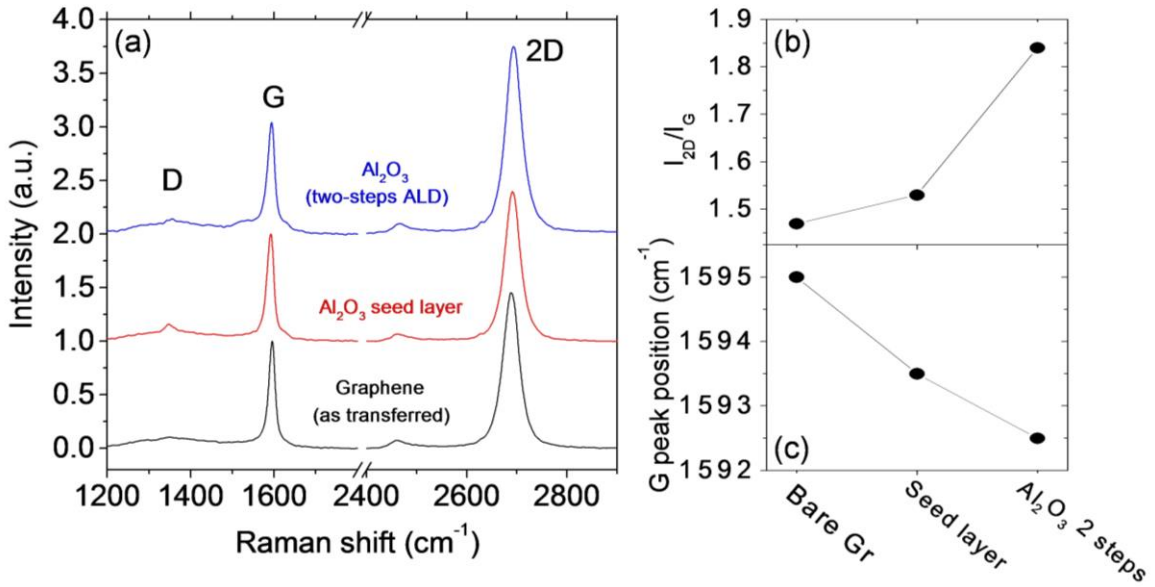

Figure 4: (a) Raman spectra of as-transferred Gr (black), after the Al_2O_3 seed layer deposition at 100 °C (red) and after the two-steps ALD deposition (blue). Behaviour of the 2D over G peak intensity ratio I_{2D}/I_G (b) and of the G peak position (c) on the three different samples.

2. Electrical characterization

2.1 Effect of Al_2O_3 deposition process on graphene sheet resistance

Transmission Line Model (TLM) patterns were electrically tested before and after the Al_2O_3 deposition (see schematics in the inserts of Fig. 5(a) and (b), respectively), in order to evaluate the impact of this process on the Gr sheet resistance $R_{sh.}$ The current-voltage (I-V) characteristics measured before the Al_2O_3 deposition between pairs of adjacent contacts with increasing spacing d from 5 to 25 μm are reported in the insert of Fig. 5(a), showing an Ohmic behaviour in the considered bias range. Fig. 5(a) reports the total resistance R_T extracted from the slope of the I-V characteristics vs d. Each experimental point is the average R_T value evaluated from 10 TLM devices and the error bar is the standard deviation. The measured resistance R_T can be related to the Gr sheet resistance and to the specific contact resistance ρ_C of the Ni pads onto Gr according to the following equation:

$$R_T = 2\left(\frac{\rho_C}{W}\right) + \left(\frac{R_{sh}}{W}\right)d \qquad (1)$$

where W is the pads width. Hence, it is possible to extract R_{sh} and ρ_c from the linear fit of the R_T vs d plot. In the case of bare Gr, R_{sh} = 320 ± 21 Ω/sq and ρ_c = 3.8 ± 0.3 Ω mm were evaluated.

Fig. 5(b) reports R_T vs d after the two-steps ALD growth of Al_2O_3. Following the same approach, the new values of R_{sh} = 1085 ± 79 Ω/sq and ρ_c = 2.6 ± 0.9 Ω mm have been calculated. The lower ρ_c after the dielectric deposition can be explained by an improved Gr/metal interface quality after the thermal annealing at 250°C occurring during the ALD process. Furthermore, the more than threefold increase of R_{sh} can be mainly attributed to a decrease of Gr carrier density (i.e., a reduced p-type doping), which is consistent with the results of Raman spectroscopy reported in the previous section. Under the present experimental conditions of a monolayer Gr encapsulated between two Al_2O_3 layers, it is expected that the two main limiting mechanisms for Gr mobility are: (i) Coulomb scattering by charged impurities and (ii) resonant

scattering by defects in the Gr lattice. [21,22] Since Raman analyses indicate that the ALD process does not introduce additional defects in Gr, a degradation of Gr mobility by the increase of defects scattering can be excluded. On the other hand, Gr mobility can be affected by trapped charges at the Gr/Al_2O_3 interface, as discussed later on.

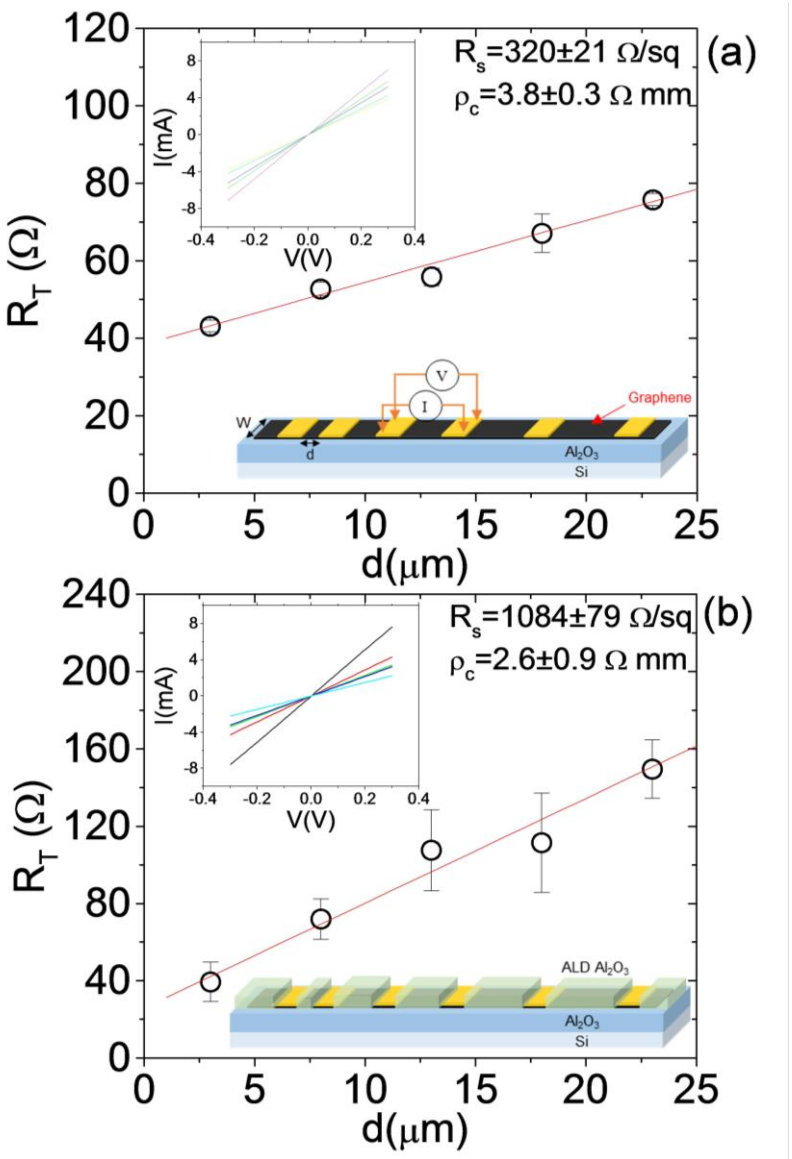

Figure 5: Total resistance R_T as a function of contacts separation d measured on TLM patterns fabricated on bare Gr (a) and after ALD growth of Al_2O_3 (b). The I-V characteristics measured between difference pairs of adjacent contacts are shown in the inserts of panels (a) and (b). Schematic illustrations of the TLM devices are also reported.

2.2 Dielectric properties of Al_2O_3 thin film on graphene

In the following the electrical properties (leakage current, breakdown field, dielectric permittivity, interface trapped charges) of the deposited Al_2O_3 dielectric film on Gr are investigated using both nanoscale current measurements by CAFM and electrical characterization (I-V and C-V) of Gr field effect transistors (GFETs).

CAFM is a non-invasive method to evaluate the electrical uniformity (in terms of current leakage) of the thin dielectric film deposited on Gr. A schematic representation of the experimental setup used for CAFM measurements is reported in Fig. 6(a). The Pt coated AFM tip is scanned in torsion resonant mode on the Al_2O_3 surface, while a DC bias is applied to the Ni/Au metal contact onto Gr. A high sensitivity current sensor records the current flowing through Al_2O_3 for each tip

position, resulting in a current map collected simultaneously to the surface morphology. CAFM measurements have been carried out both on a Gr sample with the ~4 nm thick Al_2O_3 seed layer deposited at 100 °C (Fig. 6(b) and (c)) and on the final ~22 nm thick film obtained by the two steps ALD growth (Fig. 6(d) and (e)). DC bias values of -1.5 V and -8 V have been applied to the two samples, respectively, corresponding approximately to the same electric field (~3.5 MV/cm) across the dielectric. In spite of its continuous morphology, the seed layer was found to be conductive, due to the insufficient structural quality related to the low growth temperature. Noteworthy, the highest current values through the seed layer are concentrated in the Gr wrinkles regions, probably due to a locally increased electric field associated to the nanoscale surface curvature. On the other hand, no current leakage (above the instrument noise level) is observed in the case of the 22 nm Al_2O_3 film deposited by the two-steps ALD process.

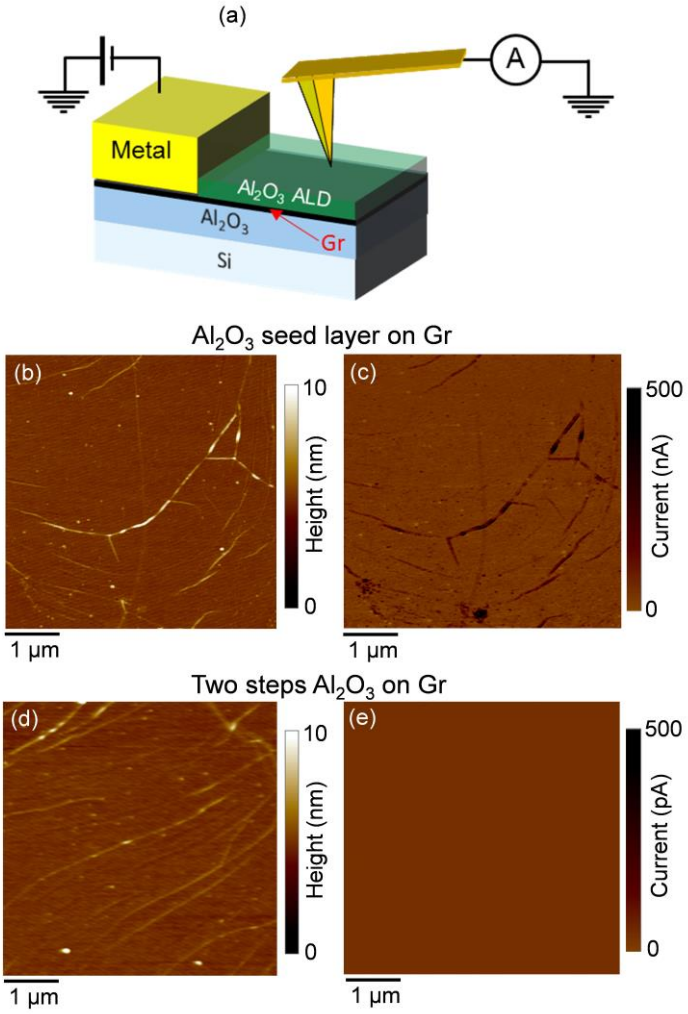

Figure 6: (a) Schematic of the CAFM setup for mapping of leakage current through the dielectric on Gr. Morphology (b) and current map (c) on the ~4 nm thick Al_2O_3 seed layer, with an applied sample bias of -1.5 V. Morphology (d) and current map (e) on the final 22 nm thick film deposited by the two steps ALD process, with an applied sample bias of -8 V.

The schematic representation of a GFET are reported in Fig. 7(a), where the relevant device geometrical parameters, i.e., the channel length L_{ch} and width W, and the length of the access regions L_{acc} between source/drain contacts and the channel have been indicated. An optical microscopy of an array of GFETs with different L_{ch} and W is reported in Fig. 7(b). Fig. 7(c) shows two representative transfer characteristics (drain current I_D vs top gate bias V_{TG}) measured at a fixed

drain bias V_{DS}=0.3 V and sweeping V_{TG} first from -5 to 5V (black curve) and then backwards from 5 to -5 V (red curve). In addition, the measured gate leakage current during the forward gate bias sweep is reported in Fig. 7(d), showing a very low current level (few pA), which demonstrates good insulating properties of the gate dielectric.

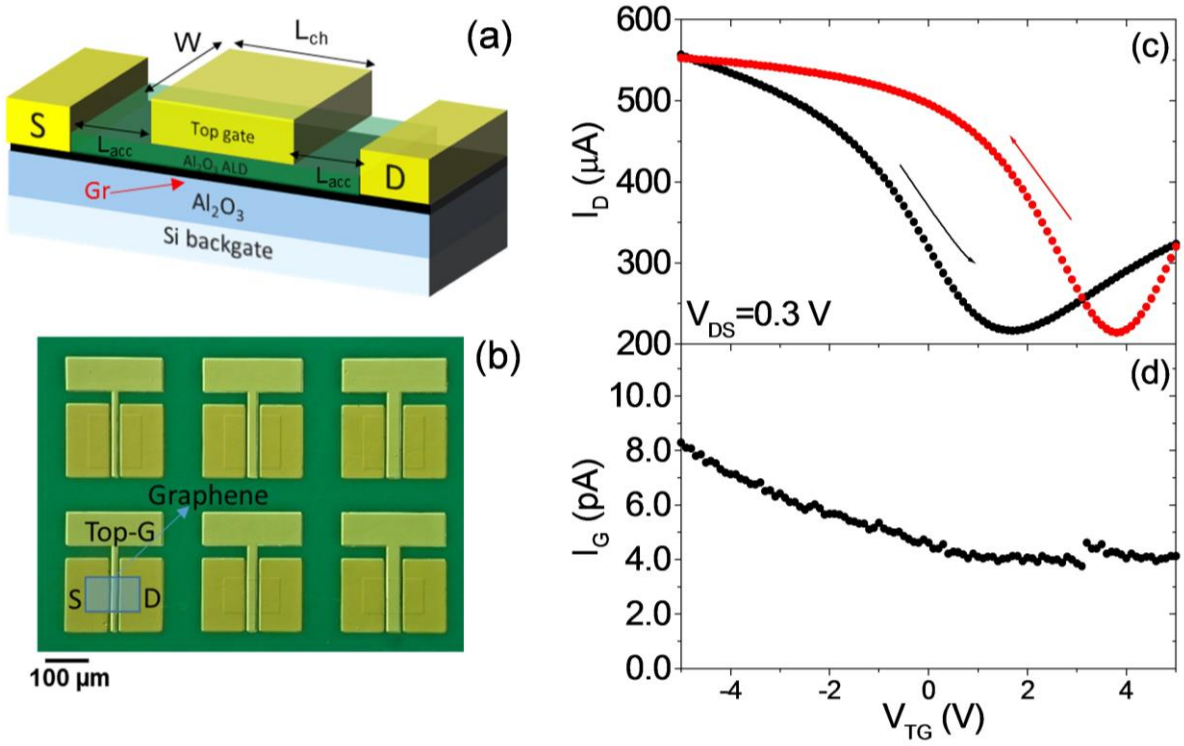

Figure 7: (a) Schematic representation of a GFET and (b) optical microscopy of an array of GFETs with different channel length and widths. (c) Representative drain current I_D vs top-gate bias V_{TG} characteristics measured with a fixed drain bias V_{DS}=0.3 V and by forward sweep of V_{TG} from -5 to 5 V (black curve) and backward sweep from 5 to -5 V (red curve). (d) Gate leakage current I_G vs V_{TG} .in the same bias range.

Both curves in Fig. 7(c) show the typical ambipolar behaviour of Gr with a current minimum occurring at the neutrality point V_D. The positive value of V_D in the first sweep (V_D=1.7 V) is related to the unintentional p-type doping of Gr. Furthermore, a hysteresis between the two I_D-V_{TG} characteristics is observed, with a positive shift ΔV_D=2.1 V of the neutrality point in the curve collected during the second (backward) gate voltage sweep, which can be ascribed to negative charge trapping at Gr-dielectric interfaces. Such hysteresis behaviour of the GFETs transfer characteristics is a commonly observed phenomenon, which can be ascribed to several factors, including charge transfer from/to ambient molecules (e.g., water and oxygen) adsorbed on the Gr surface [23] and charge trapping by defect states of the dielectric material located at the interface or near the interface with the Gr channel. [24] While the effect of ambient contaminations can be mitigated by thermal annealing treatments and by performing the measurements in vacuum or inert gas ambient, charge trapping interface states with high-k dielectric materials is an inherent problem that affects the ultimate performances of Gr devices.

First, the insulator permittivity ε, another key physical parameter of the thin dielectric film on Gr, must be evaluated. To do this we adopted the method discussed by Kim et al., [7] which is an effective approach to extract ε from DC measurements of the transfer characteristics in GFETs with both top and back-gate electrodes. In the present case, the Si substrate with the ~97 nm Al_2O_3 film worked as global back-gate, which allows to modulate the carrier density in Gr both in the channel and in the access regions.

In Fig. 8(a) the total resistance $R_T=V_{DS}/I_D$ measured between the source and drain contacts (with V_{DS}=0.3 V) is reported as a function of V_{TG}. The five different characteristics have been obtained for five fixed positive back-gate bias values from V_{BG}=0 to 10 V. Increasing the value of V_{BG} causes a shift of the Gr Fermi level towards the conduction band, resulting in a negative shift of the Dirac point position (V_D) of the R_T vs V_{TG} characteristics. Here, the neutrality point V_D shifts from 1.7 V to -0.1 V by increasing V_{BG} from 0 to 10 V. Fig. 8(b) reports the behaviour of V_D as a function $V_{BG,}$ evaluated from the transfer characteristics measured on a set of ten GFETs (the symbols are the average V_D values and the error bars the standard deviation).

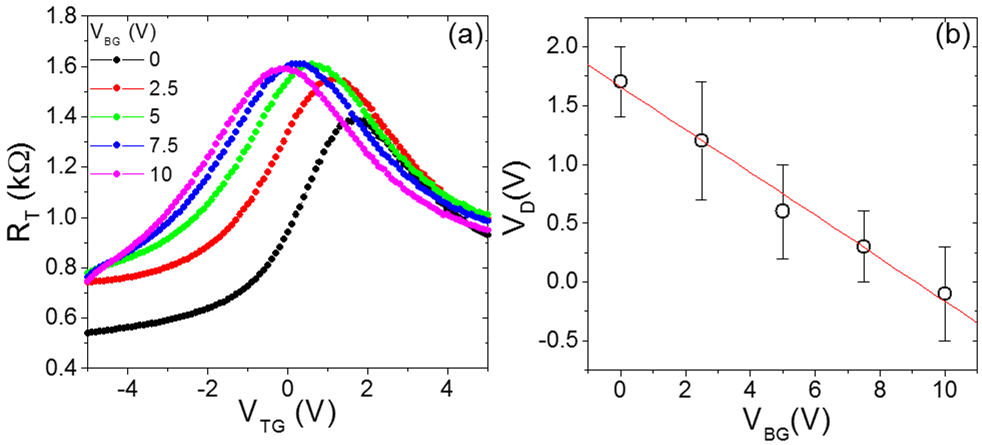

Figure 8: (a) Total resistance $R_T=V_{DS}/I_D$ between source and drain contacts as a function of V_{TG} for different for different global back-gate values (V_{BG} from 0 to 10 V). (b) Plot of the neutrality point position (V_D) as a function of V_{BG}.

According to the Gauss law, the electric field in the top-gate dielectric (V_D/d_{TG}) and that in the back-gate dielectric (V_{BG}/d_{BG}) are related to the positive charge density qn_d in the Gr layer sandwiched between the two insulating films by the following relation:

$$\left(\frac{V_D}{d_{TG}}\right)\varepsilon_{TG}-\left(\frac{V_{BG}}{d_{BG}}\right)\varepsilon_{BG}=\frac{qn_d}{\varepsilon_0} \qquad (2),$$

where d_{TG} and ε_{TG} are thickness and relative permittivity for the top-gate dielectric, whereas d_{BG} and ε_{BG} are those for the back-gate insulator. Since the top-gate and back-gate capacitance can be expressed as $C_{TG}=\varepsilon_0\varepsilon_{TG}/d_{TG}$ and $C_{BG}=\varepsilon_0\varepsilon_{BG}/d_{BG}$, the following linear relation between V_D and V_{BG} can be derived from Eq. (2):

$$V_D=\left(\frac{C_{BG}}{C_{TG}}\right)V_{BG}+\frac{qn_d}{C_{TG}} \qquad (3)$$

Hence, the ratio C_{BG}/C_{TG}=0.19±0.01 can be obtained as the slope of the linear fit of the experimental data in Fig. 8(b). The capacitance C_{BG} of the Al_2O_3 back gate dielectric with thickness d_{BG}=97 ± 0.1 nm thick Al_2O_3 film on the Si substrate was preliminarily evaluated by C-V analyses with a mercury probe, revealing a dielectric constant of ε_{BG}=6.25 ± 0.01. Hence, the top gate capacitance C_{TG} calculated from the slope of the linear fit is 0.30±0.02 μF cm^{-2}, from which a dielectric constant of ε_{TG} = 7.45 ± 0.7 was obtained considering a thickness of 22 nm for the Al_2O_3 film deposited by the two-steps ALD on Gr. Noteworthy, this permittivity value is very close to the value (7.53 ± 0.3) measured by C-V on an Al_2O_3 thin film deposited with the same ALD process on a Si reference sample (see Fig.S3, Supporting information).

After evaluating the permittivity of the dielectric film on Gr, charge trapping phenomena by interface and/or near interface states of the Al_2O_3 were investigated. To this aim, high frequency (1Mz) capacitance-voltage measurements have been

performed on the same GFET structure illustrated in Fig. 7(a), by applying the bias to the top gate dielectric and grounding the source, drain and back-gate contacts. Parasitic capacitance values have been subtracted by performing a measurement on an identical FET structure without Gr. Fig. 9(a) shows the results of C-V measurements carried out by sweeping V_{TG} from negative to positive values (circles) and backwards (triangles), using progressively increasing sweep range from -1 to 1V to -5 to 5 V.

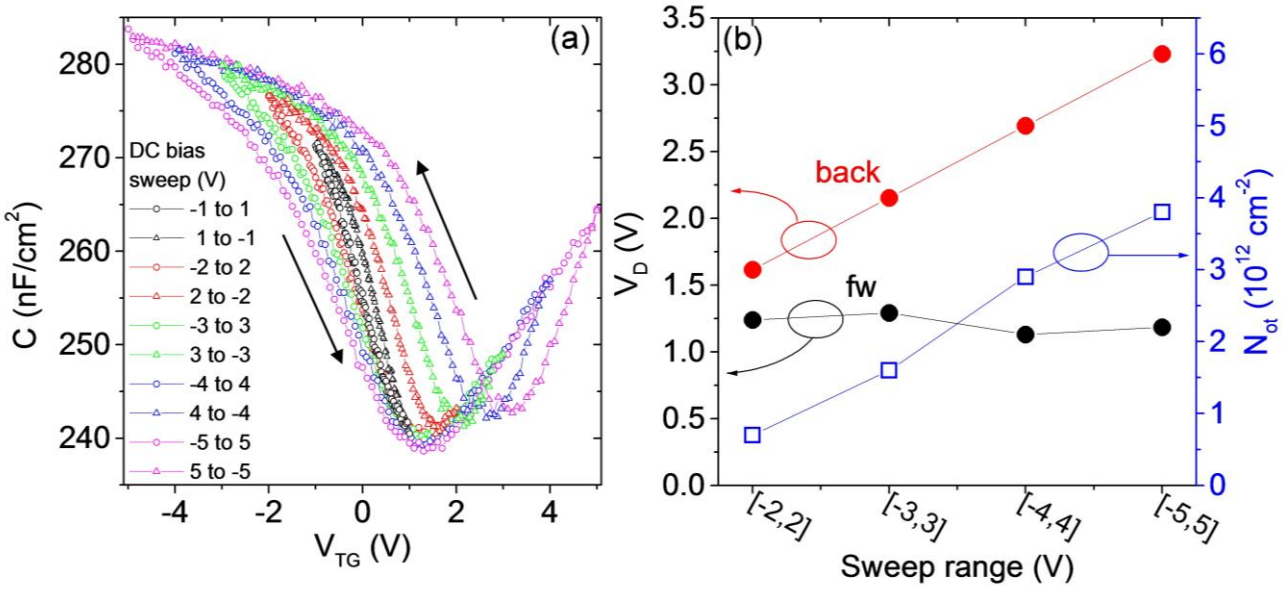

Figure 9: (a) C-V measurements performed at 1 MHz frequency by sweeping the top-gate bias V_{TG} from negative to positive values (circles) and backwards (triangles), using progressively increasing sweep range: -1 to 1V and back (black symbols), -2 to 2 V and back (red symbols), -3 to 3 V and back (green symbols), -4 to 4 V and back (blue symbols), and -5 to 5 V and back (violet symbols). (b) Neutrality point position V_D (left axis) as a function of the bias sweep range for the forward (black dots) and backward sweep (red dots). The trapped charges density N_{ot} by near interface oxide traps is reported on the right axis.

The following interesting aspects can be deduced by these C-V analyses. (i) The neutrality point V_D remains in the same position in the forward bias sweep with increasing the sweep range, whereas it is progressively shifted towards positive bias values in the backward sweep. (ii) The C-V characteristics exhibit an increasing stretching along the V_{TG} axis with increasing the sweep bias range.

All these aspects can be explained in terms of trapping/detrapping of the Gr free carriers (holes and electrons) by Al_2O_3 trap states located at the interface or near the interface with the Gr. Clearly, these trapping states exhibit different characteristic/discharging times, i.e., the interface traps can be able to exchange rapidly charges with the Gr two-dimensional-electron-gas (2DEG) during the sweep, whereas the near interface traps (located within the dielectric at nanometric distance from Gr) typically retain the trapped charges for longer times. Fig. 9(b) shows the neutrality point position as a function of the sweep bias range for the forward (black dots) and backward sweep (red dots). The neutrality point $V_{D,fw}$ during each forward bias sweep does not depend on the initial negative bias value, indicating a negligible trapping of holes in the oxide near interface region for $V_{TG}<V_{D,fw}$ (when holes are accumulated at the interface). The value of $V_{D,fw}$ is determined by the unintentional p-type doping of Gr. On the contrary, for $V_{TG}>V_{D,fw}$ electrons are accumulated at the interface and can be trapped in the oxide. This negative charge is retained during the subsequent backward sweep, causing a positive shift of the neutrality point $V_{D,bk.}$ and it is finally discharged for $V_{TG}<V_{D,bk}$. The electron trapping effect

in the forward sweep increases linearly with increasing the sweep range, as shown in Fig. 9(b). The negative charge density retained by near-interface oxide traps, calculated as

$$N_{ot} = \frac{C_{TG}}{q}\left(V_{D,bk} - V_{D,fw}\right) \qquad (4)$$

is reported on the right vertical axis of Fig. 9(b).

While the positive shift of the neutrality point between backward and forward bias sweep is due to charge trapping by near-interface oxide traps, the stretching of the C-V characteristics along the bias axis can be associated to the total interface charge density N_t trapped by both interface and near-interface traps. N_t can be extracted by fitting of the C-V characteristics in Fig. 9(a).

The two main contributions to the GFET capacitance are represented by the constant capacitance C_{TG} of the Al_2O_3 top-gate dielectric in series with the bias dependent quantum capacitance contribution C_q of the Gr channel, which accounts for the dependence of the Gr density of states on the Fermi level position. [25,26] C_q can be expressed as a function of the Gr carrier density n as: [25]

$$C_q = \frac{2q^2}{2\hbar v_F \sqrt{\pi}} \sqrt{|n| + |n^*|}, \qquad (5)$$

where v_F is the Gr Fermi velocity (v_F=1×10^6 m/s), ħ is the reduced Planck's constant, and n* is an "effective" charged impurities concentration that determines the minimum value of C_q at the neutrality point. This impurities concentration accounts for the effects of disorder close to the Dirac point, i.e., the occurrence of local potential fluctuations and electron-hole puddles in Gr. [27,28]

The presence of trapping states at the interface with the dielectric gives rise to an additional capacitive contribution C_{it} in parallel to C_q. This term C_{it} depends on the measurement frequency ω. For a high frequency modulation during C-V measurements, interface traps are not fast enough to exchange charge with the Gr 2DEG and C_{it} becomes negligible. As a matter of fact, the traps times constants for Gr capacitors with Al_2O_3 dielectrics reported in the literature are typically ranging from tens of μs to ms, [29] although faster states with time constant of 0.3 μs have been also recently revealed. [30] This means that the 1 MHz frequency used in our C-V measurements can be high enough to neglect the parallel capacitance contribution C_{it}. Hence, the measured capacitance can be modelled as:

$$C = \frac{C_{TG}C_q}{C_{TG} + C_q}. \qquad (6)$$

On the other hand, the DC bias sweep applied during C-V measurements is slow enough that interface traps can cause a stretching of the C-V characteristics along the voltage axis. In the ideal case of a Gr/dielectric system free of interface traps, the Gr Fermi level position E_F with respect to the Dirac point is related to the point top-gate bias $V_{TG,id}$ as:

$$V_{TG,id} - V_D = E_F + \frac{q^2}{\pi\hbar^2 v_F^2 C_{TG}} E_F^2 \qquad (7)$$

In the presence of interface traps, V_{TG}–V_D results to be increased with respect to $V_{TG,id}$-V_D as follows:

$$V_{TG} - V_D = V_{TG,id} - V_D + \frac{qN_t(E_F)}{C_{TG}}, \qquad (8)$$

where $N_t(E_F)$ is the total density of interface trapped charges as a function of the Fermi level position. In the following, the fitting procedure to evaluate $N_t(E_F)$ from the measured high frequency C-V characteristics is illustrated.

In Fig. 10 the capacitance measured during the forward bias sweep from -5 to 5V (a) and the subsequent backward sweep from 5 to -5 V (b) is reported as a function of V_{TG}-V_D. As a reference, the top-gate dielectric capacitance C_{TG} is reported as blue dashed line in the same figures. The C vs V_{TG} curve in the ideal case of zero interface traps, calculated using Eqs (5) and (6) and (7) is reported as green line in Figs 10(a) and (b). The value of n* in the expression of C_q has been fixed to obtain the same minimum capacitance value in the ideal C-V curve as in the experimental one. Fig. 10(c) reports (green line) the dependence of $V_{TG,id}$-V_D on E_F obtained from Eq.(7), whereas the behaviour of V_{TG}-V_D on E_F, evaluated from the stretching along the voltage axis of the experimental C-V curves with respect to ideal ones, is shown in the same figure by black and red dots for the forward and backward sweeps, respectively. The trapped charges N_t as a function of E_F in the forward and backward sweeps, evaluated according to Eq.(8), are reported in Fig. 10(d). Finally, the C-V curves calculated by Eqs. (5), (6) and (8), using the N_t profile in Fig. 10(d) are reported in Fig. 10(a) and (b) as red lines, showing a good fitting with experimental data.

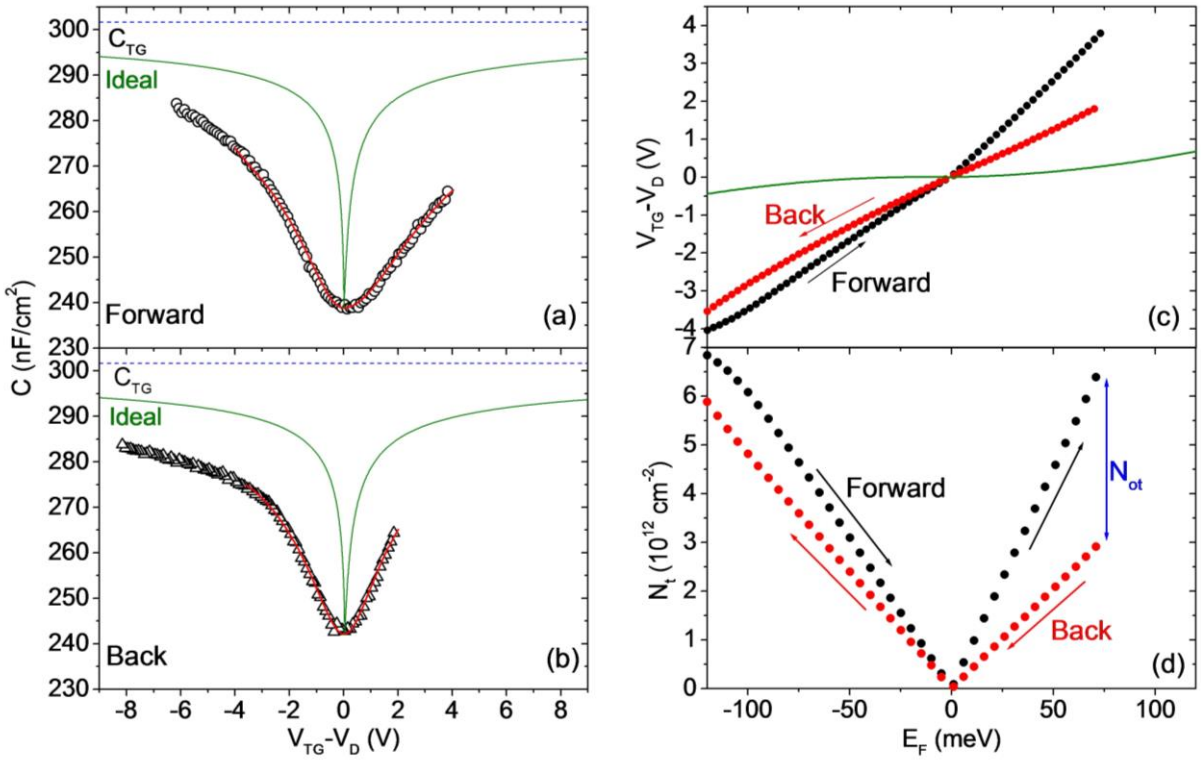

Figure 10: Measured capacitance C vs V_{TG}-V_D characteristics during the forward bias sweep from -5 to 5V (a) and the backward sweep from 5 to -5 V (b), compared with the calculated C vs V_{TG}-V_D in the ideal case of zero interface states (green line) and with the top-gate dielectric capacitance C_{TG} (blue dashed line). (c) Ideal (green line) and experimental dependence of (V_{TG}-V_D) on E_F for the forward (black dots) and backward bias sweep (red dots). (d) Evaluated total density of interface trapped charges N_t as a function of E_F in the forward (black dots) and backward sweep (red dots).

In the forward bias sweep, a nearly linear decrease of N_t with E_F is first observed for decreasing negative values of E_F, indicating detrapping of holes from the interface traps. A linear increase of N_t with E_F is therefore observed for positive shifts of the Fermi level, indicating electron trapping in the interface traps. When the bias sweep is inverted (red dots), a fraction of trapped electrons are not immediately released, giving rise to a lower N_t than in the forward sweep. It is worth noting that the difference between the N_t values at the end of the forward sweep and at the beginning of the backward one

(indicated by a vertical blue line), corresponds approximately to the near interface trapped charge N_{ot} previously estimated (see Fig. 9(b)).

By repeating the same fitting procedure for all the C-V characteristics reported in Fig. 9(a), the behaviour of $N_t(E_F)$ for the different DC bias sweeps was evaluated, as shown in Fig. 11(a)-(e). While N_t vs E_F profiles are nearly identical for the forward and backward sweep in the -1 to 1 V bias range, the spread between the two profiles becomes increasingly higher for larger sweep ranges.

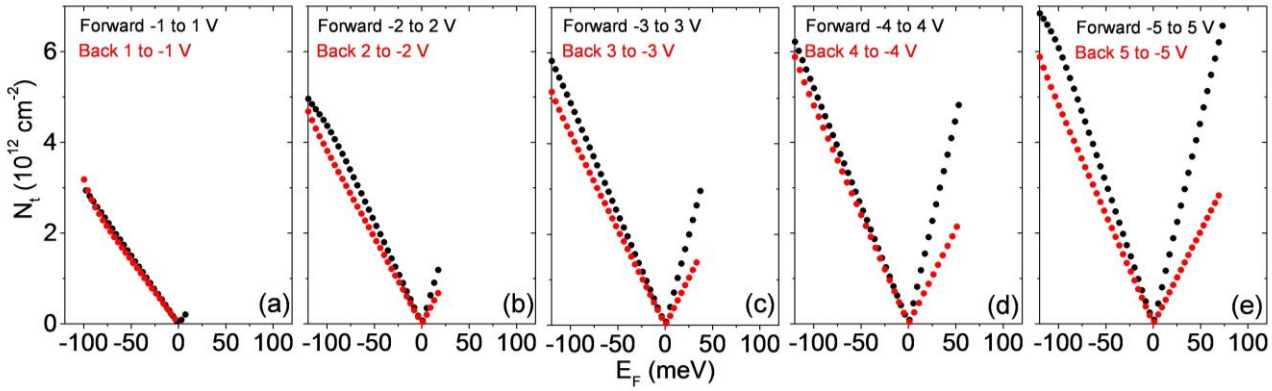

Figure 11: Evaluated total density of interface trapped charges N_t as a function of E_F in the forward (black dots) and backward sweep (red dots) for the sweeping ranges from -1 to 1 V (a), -2 to 2 V (b), -3 to 3 V (c), -4 to 4 V (d), -5 to 5 V (e).

Finally, the breakdown electric field of the Al_2O_3 top gate dielectric was estimated. This is illustrated in Fig. 12, showing the gate leakage current for a representative GFET device a function of the V_{TG}-V_D (bottom horizontal scale). A drain bias V_{DS}=0.3 V is applied during this measurement and the drain current I_D is simultaneously acquired. Noteworthy, I_G only slightly increases from 10 to 100 pA in the bias range from 0 to ~16 V, whereas a sudden current increase by more than 4 orders of magnitude is observed at 16.3 V, which is accompanied by a drop of I_D in the transfer characteristic. This indicate the occurrence of a non-reversible failure of the device, which can be associated to the top dielectric, as we verified that current still flows between source and drain for V_{TG}=0 V. The electric field $E=(V_{TG}-V_D)/d_{TG}$ across the top gate dielectric has been reported on the top horizontal scale in Fig. 12, showing a dielectric breakdown field E_{BD}=7.4 MV/cm.

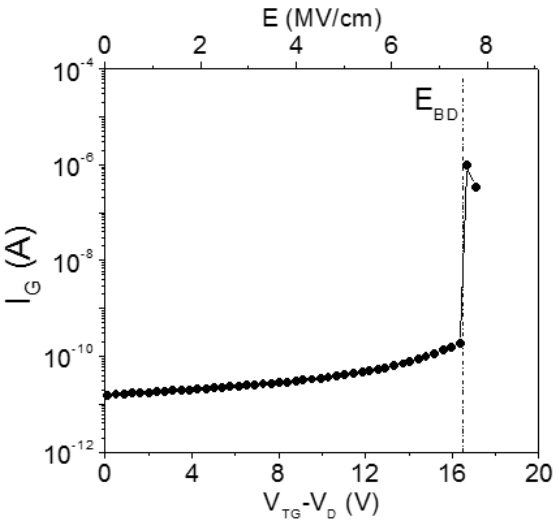

Figure 12: Gate leakage current I_G of a GFET as a function of V_{TG}-V_D (bottom horizontal axis) and of the electric field across the top gate oxide (top axis). A dielectric breakdown field of 7.4 MV/cm is indicated by the vertical dashed line.

2.3 Transconductance and field effect mobility

Finally, the transconductance and the mobility were evaluated from the transfer characteristics of top gated GFETs with different channel lengths. In order to estimate the intrinsic transconductance of the device, the channel resistance R_{ch} was extracted from the measured total resistance R_T by subtracting the series resistance contributions, i.e., (i) the contact resistances (R_c) of the Ni/Au source and drain contacts onto Gr and (ii) the access resistances (R_{acc}) of the two access regions between source and drain contacts and the channel region. The R_c and R_{acc} contributions could be evaluated from the specific contact resistance and Gr sheet resistance obtained by TLM analyses reported in Fig. 5. Hence, R_{ch} was extracted as follows:

$$R_{ch} = R_T - \left(2\frac{\rho_c}{W} + 2R_{sh}\frac{L_{acc}}{W} \right) \qquad (9)$$

where W=100 µm is the channel width and L_{acc}=6.5 µm is length of each access region.

Figure 13(a) (black line) reports the R_{ch} vs V_{TG} for a GFET with channel length L_{ch}=15 µm. The intrinsic channel transconductance $g_{m,i}$, was calculated as:

$$g_{m,i} = V_{DS}\frac{d}{dV_{TG}}\left(\frac{1}{R_{ch}}\right) \qquad (10)$$

The behaviour of $g_{m,i}/W$ is reported as blue line in Fig. 13(a), right vertical axis. The minimum value of $g_{m,i}$ (at $V_{TG}\approx$-1 V) corresponds to the peak hole transconductance. Fig. 13(b) reports the peak value of the hole transconductance measured on devices with different channel lengths L_{ch} from 15 to 45 µm, showing a decrease of $g_{m,i}/W$ as a function of L_{ch}. The transconductance is expected to be proportional to $1/L_{ch}$ according to the following relation: [31]

$$\frac{g_{m,i}}{W} = \frac{1}{L_{ch}}\mu_{FE}C_{TG}V_D \qquad (11)$$

being μ_{FE} the hole field effect mobility. Fitting the experimental data with Eq.(12), a value of μ_{FE}= 1173 ± 27 $cm^2V^{-1}s^{-1}$ was estimated.

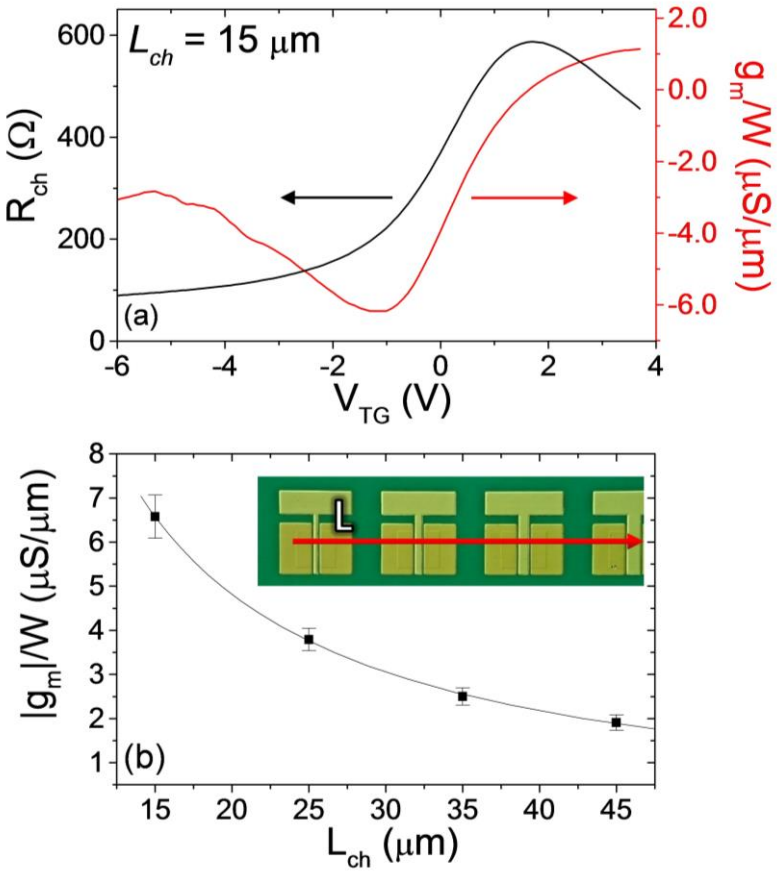

Figure 13: (a) Channel resistance R_{ch} vs V_{TG} for a GFET with 15 µm channel length (black line and left vertical axis) and corresponding intrinsic transconductance $g_{m,i}/W$ (red line and right vertical axis). (b) Peak hole transconductance $|g_{m,i}/W|$ measured on GFETs with different channel lengths L_{ch} and fit of experimental data. An optical image of an array of GFETs with different L_{ch} is shown as insert.

Conclusion

In conclusion, a detailed morphological, structural and electrical investigation of Al_2O_3 thin films grown on large area Gr residing on an Al_2O_3/Si substrate by a two-steps ALD process (H_2O-assisted seed later deposition at 100 °C, followed by ALD deposition at 250 °C) has been reported. Optimization of the low temperature seed layer deposition step allowed to obtain a uniform, conformal and pinhole-free Al_2O_3 film on the Gr membrane. Nanoscale resolution mapping of the current through the dielectric by conductive AFM demonstrated a laterally uniform film with negligible leakage current for the typical gate electric fields applied during transistor's operation. Raman spectroscopy measurements indicated that the ALD process does not introduce defects in Gr, whereas it produces a partial compensation of unintentional p-type doping. This was confirmed by the increase of Gr sheet resistance after the ALD deposition evaluated by electrical characterization of TLM test structure. Current-voltage characterization of GFETs allowed to evaluate the relative dielectric permittivity (ε=7.45) and the breakdown electric field (E_{BD}=7.4 MV/cm) of the Al_2O_3 film on Gr, as well as the transconductance and the holes field effect mobility (~1200 $cm^2V^{-1}s^{-1}$). Finally, high frequency capacitance-voltage measurements on the transistors were used to investigate the charge trapping mechanisms due to near-interface and interface states of the dielectric, which are responsible of the hysteresis of the electrical characteristics. A reduction of

interface traps density through further optimization of the seed-layer process and/or by proper post-deposition treatments is the key to improve GFETs electrical performances. All these results can have important implications for the improvement of the Al_2O_3/Gr system for next generation electronics applications.

Supporting Information

AFM analysis of as-transferred graphene on Al_2O_3/Si.
Deposition of Al_2O_3 on graphene at 250°C without the in-situ seed layer.
Capacitance-Voltage characterization of Al_2O_3 thin films deposited by two-steps ALD on silicon substrates.

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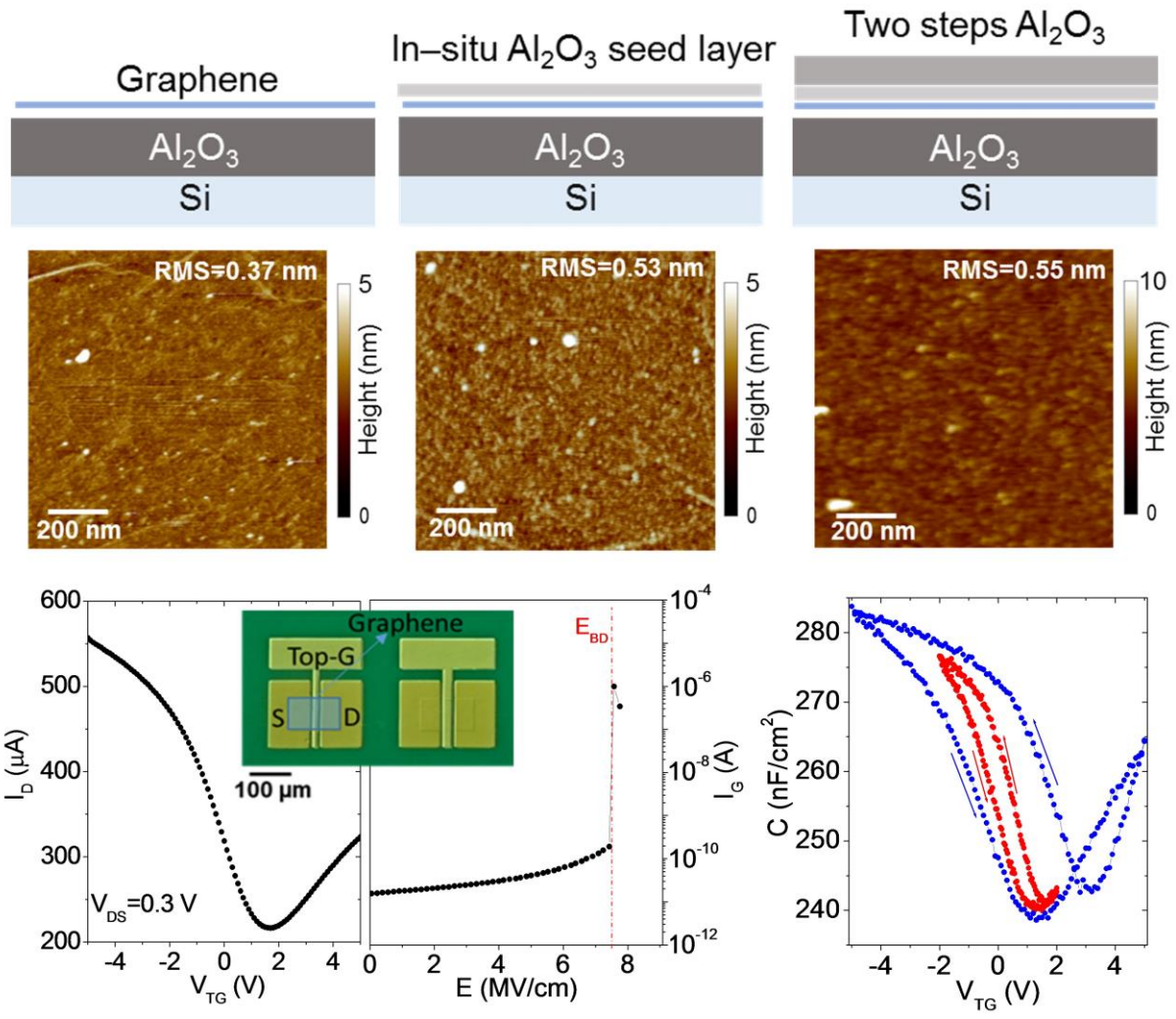

Graphic for the table of contents (TOC)